SGS-THOMSON MICROELECTRONICS

STi3400

MPEG/H.261 VIDEO DECODER

- REAL-TIME DECODING OF MPEG-1 (SIF-525/SIF-625) AND H.261 (CIF/QCIF) VIDEO BITSTREAMS
- YC_BC_R OR RGB OUTPUTS COMPATIBLE WITH PAL AND NTSC FORMAT DISPLAYS
- PROGRAMMABLE PICTURE AND DISPLAY WINDOW FORMAT
- INTEGRATED PROGRAMMABLE VIDEO TIMING GENERATOR
- HORIZONTAL AND VERTICAL FILTERS FOR PICTURE FORMAT CONVERSION
- SUPPORT FOR DISPLAY OF HIGH RESOLUTION STILL PICTURES
- AUTOMATIC MACROBLOCK ERROR CONCEALMENT
- SUPPORT FOR TRICK MODES : FAST FORWARD, REVERSE, SLOW MOTION
- STANDARD 8/16-BIT MICROCONTROLLER INTERFACE WITH DMA SUPPORT FOR COMPRESSED DATA INPUT
- SERIAL COMPRESSED DATA PORT OPTION
- MAXIMUM POWER DISSIPATION 0.6W

APPLICATIONS

- CD-I/VIDEO CD DECODER
- MULTIMEDIA PC
- VIDEO CONFERENCING SYSTEM

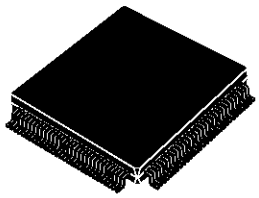
DESCRIPTION

The STi3400 is a real-time video decompression processor supporting the MPEG-1 and H.261 standards at the SIF or CIF picture formats. The digital video output can be formatted for PAL or NTSC type interlaced displays. The complete decoding function is realised with the STi3400, a standard 8-bit or 16-bit microcontroller and a bank of DRAM memory. A typical memory configuration is a single 256K x 16 DRAM. Up to 32 Mbits of memory can be addressed.

The STi3400 requires minimal support from an external microcontroller, which is mainly required to initialize the decoder at the start of every picture. To aid the external processing of the upper layers of compressed video bitstream syntax, a start code detector is provided on the chip. In addition, a register is provided to allow the tracking of time-stamps.

Compressed data may either be input through the microcontroller data port under program or DMA control, or through a dedicated serial port.

Undetected bitstream errors which would cause decoder errors bring into play an error concealment function, replacing the lost data with data from a previous picture.



PQFP120
(Plastic Quad Flat Pack)

ORDER CODE : STi3400

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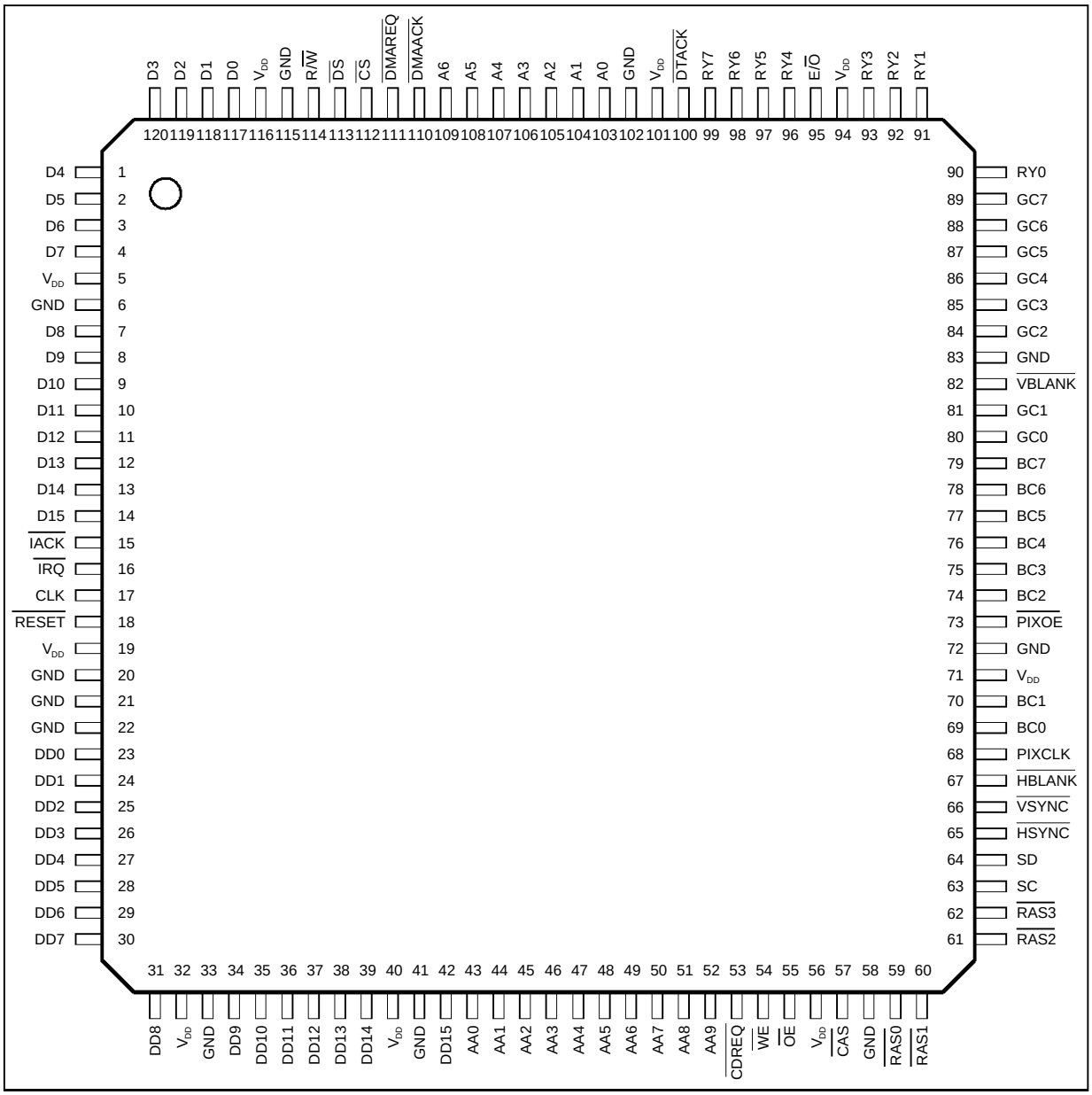
I - PIN DESCRIPTION

I.1 - Pin Connections



I - PIN DESCRIPTION (continued)

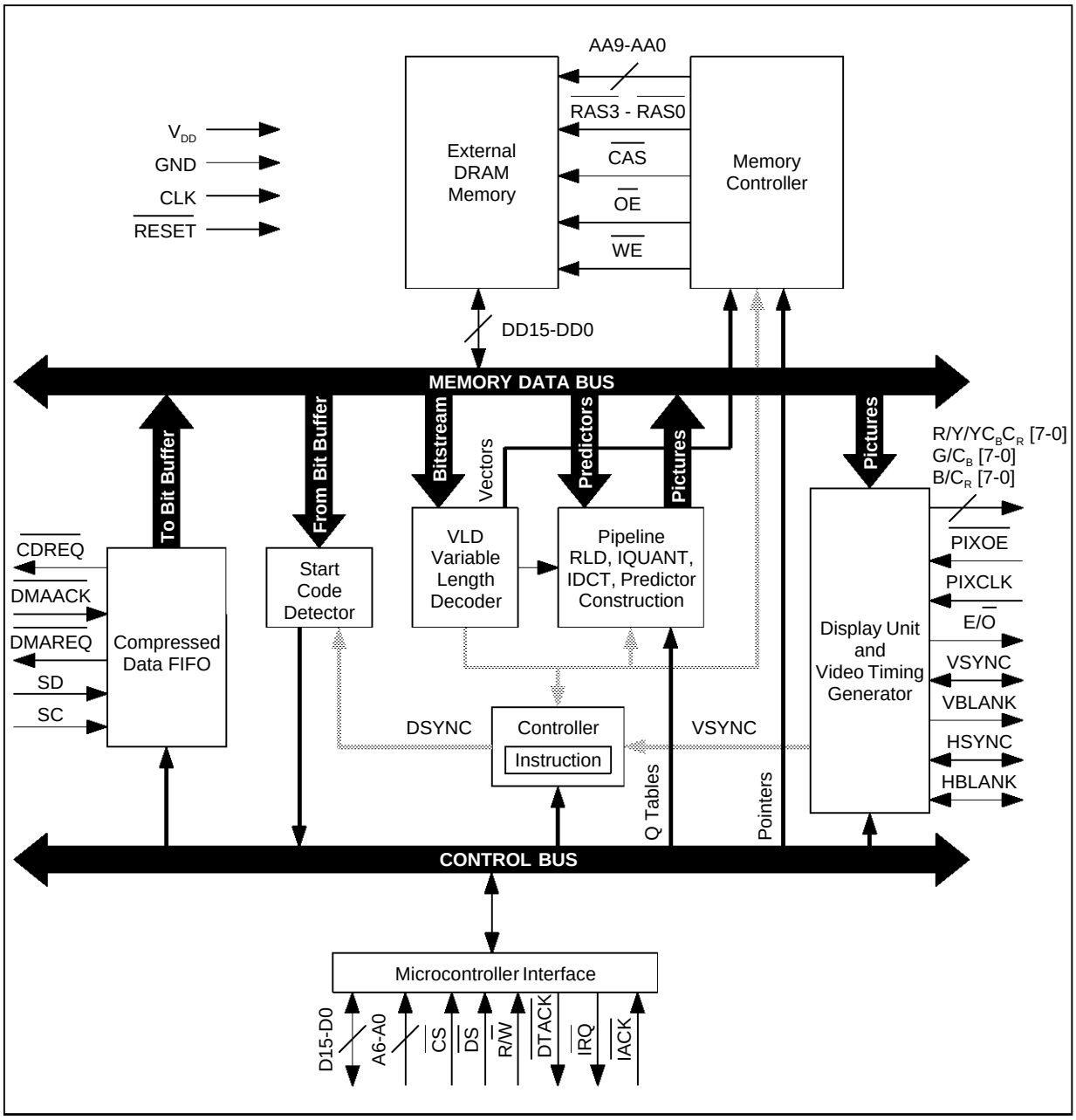
I.2 - Pin List

Pin Number	Name	Type	Function
SYSTEM SERVICES AND NON-FUNCTIONAL PINS			
5, 19, 32, 40, 56, 71, 94, 101, 116	V_{DD}		Power Supply
6, 20, 33, 41, 58, 72, 83, 102, 115	GND		Ground
17	CLK	I	System Clock
18	$\overline{\text{RESET}}$	I	Master Reset
21, 22	GND		Reserved Pins, Connect to Ground
MICROCONTROLLER INTERFACE			
14-7, 4-1, 120-117	D15 - D0	I/O	Bidirectional Data Bus
109-103	A6 - A0	I	Address
112	$\overline{\text{CS}}$	I	Chip Select
113	$\overline{\text{DS}}$	I	Data Strobe
114	R/$\overline{\text{W}}$	I	Read/Write Selection
100	$\overline{\text{DTACK}}$	O (open-drain)	Data Acknowledge
16	$\overline{\text{IRQ}}$	O (programmable open-drain)	Interrupt Request
15	$\overline{\text{IACK}}$	I	Interrupt Acknowledge
DRAM INTERFACE			
42, 39-34, 31-23	DD15 - DD0	I/O	Bidirectional Data Port
52-43	AA9 - AA0	O	Address
62-59	$\overline{\text{RAS3}}$-$\overline{\text{RAS0}}$	O	Row Address Strobes for Banks 3, 2, 1 and 0
57	$\overline{\text{CAS}}$	O	Column Address Strobe
55	$\overline{\text{OE}}$	O	Output Enable
54	$\overline{\text{WE}}$	O	Write Enable
VIDEO INTERFACE			
99-96, 93-90	RY7 - RY0	O	R or Y Video Port or Multiplexed Y/C_B/C_R
89-84, 81, 80	GC7 - GC0	O	G or C_B Video Port
79-74, 70, 69	BC7 - BC0	O	B, C_R or Multiplexed C_B/C_R Video Port
68	PIXCLK	I	Pel Clock
73	$\overline{\text{PIXOE}}$	I	Video Port Output Enable
95	E/$\overline{\text{O}}$	I/O (see Note)	Even/Odd Field Selection
66	$\overline{\text{VSYNC}}$	I/O (see Note)	Vertical or Composite Sync
82	$\overline{\text{VBLANK}}$	O (see Note)	Vertical or Composite Blanking
65	$\overline{\text{HSYNC}}$	I/O (see Note)	Horizontal Sync
67	$\overline{\text{HBLANK}}$	I/O (see Note)	Horizontal Blanking (out) /Composite Blanking (in)
COMPRESSED DATA INPUT CONTROL			
53	$\overline{\text{CDREQ}}$	O	Compressed Data Request
110	$\overline{\text{DMAACK}}$	I	DMA Acknowledge
111	$\overline{\text{DMAREQ}}$	O (programmable open-drain)	DMA Ready (request)
64	SD	I	Serial Port Data
63	SC	I	Serial Port Clock

Note : Polarity programmable

II - BLOCK DIAGRAM

Figure 1 : General Block Diagram



III - FUNCTIONAL DESCRIPTION

III.1 - STi3400 Architecture

The functional block diagram of the STi3400 is given in Figure 1. The three external interfaces, to the microcontroller, DRAM memory and display are indicated. An STi3400, together with a minimum of 4 Mbits of DRAM, a microcontroller, and some video post processing, enables a complete video decoding system to be constructed.

The microcontroller interface has a 16-bit data bus and 7 address lines. It can be configured as an 8-bit interface if required, and can be set up to operate with either the "Intel" or the "Motorola" protocol. This access port has two functions :

- to enable control of the STi3400 by providing interrupts and a path for reading from writing to internal registers,
- to pass the compressed data, either under program or DMA control, into the bit buffer, maintained by the STi3400 in the external DRAM.

A serial port is available for use as an alternative input mode for compressed data.

The DRAM interface includes all of the signals necessary for control of the memory. Refresh is handled automatically by the STi3400. The memory is used to hold the bit buffer, and to store decoded pictures.

The video interface outputs digital video in 16 or 24-bit RGB or YC_BC_R format. Synchronization signals can either be provided externally or generated by the on-chip video timing generator.

The STi3400 has two global buses, a high speed 16-bit memory data bus, and a 16-bit control bus. All data transfers to and from the external DRAM memory pass over the memory bus. These transfers are organised as packets in order to take advantage of page-mode access to the memory. The memory controller allocates bus bandwidth to those STi3400 processes requiring memory data transfers according to a fixed priority scheme. The low bandwidth control bus is the communication path for data passing through the microcontroller interface.

During the process of decoding, the STi3400 performs four concurrent activities :

- buffering of the incoming bitstream,
- searching for start codes in the bitstream,
- decoding of a picture,
- display of a picture.

For each of these processes, the microcontroller must set up parameters and monitor events communicated by interrupts. The main features of each of these processes are summarized below.

III.1.1 - Bitstream Buffering

The STi3400 manages the bitstream buffering needed by the decoding system. The size of this buffer, which is located in the DRAM memory, is set up by the user. The bitstream is entered either through the microcontroller data bus or the serial port. The compressed data input process is asynchronous to all other processes in the STi3400. The bitstream data passes through a 512-bit internal FIFO (the compressed data FIFO) before being transferred in packets to the bitstream buffer across the memory data bus. An external signal (and associated interrupt) indicate when the FIFO is full, enabling the use of DMA for bitstream input.
The maximum continuous bitstream input rate is 20 Mbit/s through the serial port, and 10 Mword/s (of 8 or 16 bits) through the microcontroller interface.

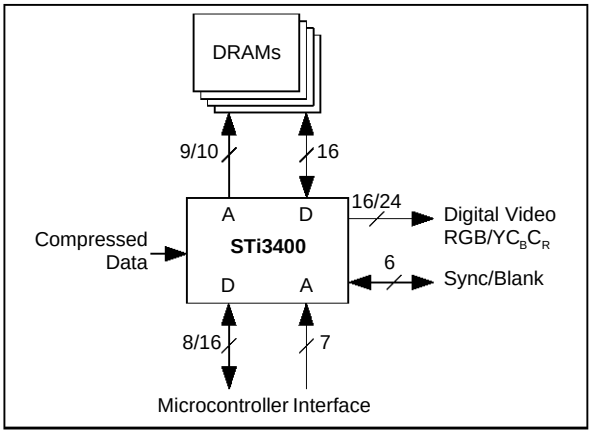
The STi3400 accepts the following types of bitstream :

- MPEG video elementary stream.
- H.261 after unframing and error correction.

III.1.2 - Start Code Search

The STi3400 is able to decode automatically a video bitstream from the slice layer downwards. The user must decode headers belonging to the higher layers (i.e. picture and upwards) in order to extract the information needed for appropriately setting up STi3400 registers and quantization tables. Since the header information requires minimal interpretation, and does not have to be examined more than once per picture, this task represents only a small load on the microcontroller. The start code detector (SCD), which operates in parallel with the decoding pipeline, parses the bitstream extracted from the bit buffer and locates start codes corresponding to picture layer and above.

Figure 2



III - FUNCTIONAL DESCRIPTION (continued)

When one of these start codes has been found, the start code detector stops and signals an interrupt. The microcontroller is then able to read from the STi3400 the header data following the start code in the bitstream. The SCD starts automatically whenever the decoding of a new picture starts and on user command. Normally, start code parsing is performed one picture in advance of decoding.

III.1.3 - Decoding

The STi3400 is a picture decoder ; it decodes a single picture and then stops until set up for the decoding of the next picture present in the video bitstream.

In the standard mode of operation, the decoding of a new picture commences simultaneously with the start of the display of a new picture. The registers whose contents need to be changed from picture to picture are double-banked and are updated automatically when decoding starts. These registers are set up during the decoding of the preceding picture.

The bitstream is read from the bit buffer into the variable-length code decoder (VLD), and into the picture reconstruction (decoding) pipeline. Any predictors required for macroblock reconstruction are fetched from the appropriate area of the external memory, and the reconstructed picture is written back into the area of this memory assigned to it by the user. The pipeline contains the following subblocks :

- predictor construction and averaging (”filter”),
- run/level decoder (RLD),
- inverse zig-zag reordering,
- inverse quantizer (IQUANT),
- inverse discrete cosine transformation (IDCT).

While a picture is being decoded the start code detector is used to locate the start of next picture header, which the microcontroller can then read in order to set up the double-banked registers for the decoding of the next picture.

III.1.4 - Display

The STi3400 is able to output digital pel data in either YC_BC_R 4:2:2/4:4:4 or RGB 4:4:4 formats, suitable for both interlaced and non-interlaced display. When displaying the decoded pictures on an interlaced display, the same data would normally be used in both fields. The STi3400 also allows the possibility of decoding and displaying high resolution still pictures, in which case different data would be output for each field.

The frame rate, which does not have to be the same as the picture decoding rate, is defined by the video timing signals. These may be input externally, or generated internally by the video timing generator (VTG). In both cases, the pel clock, PIXCLK, must be provided externally. Pel rates of up to 30MHz are possible.

The programmable VTG generates horizontal, vertical and composite synchronization and blanking signals. User-programmable registers enable all required pulse widths and polarities to be defined. Interlaced or non-interlaced mode can be programmed.

In applications where it is necessary to double the horizontal size of the decoded picture to match the display line length, an 8-tap upsampling filter is provided for both luminance and chrominance. A 2-tap vertical filter is provided for reconstruction of chrominance samples from the internal 4:2:0 format. The vertical filter includes a data delay line of length 352.

III.2 - VSYNC and DSYNC

These are the two principal internal synchronization signals of the STi3400. They will be referred to many times in the sections that follow.

VSYNC is equivalent to the video timing signal of the same name. Its source may be external or internal, if the video timing generator is enabled. VSYNC always starts the display of a new picture. It also can potentially start the decoding of a picture, since it is the primary synchronization signal of the pipeline controller (see Figure 1).

At the start of a new picture decoding task, the signal DSYNC is generated. DSYNC also launches the search for a start code. Thus the picture decoding and start code detection functions are slaved to the display. It is possible, however, for the external controller to initiate asynchronous decoding and start code detection operations if required.

III - FUNCTIONAL DESCRIPTION (continued)

III.3 - A Note on Conventions

In this Data Sheet, the following conventions are used when documenting the functions of signals :

- I/O signals can either be active high or active low. The former have names without an overbar (i.e. SIGNAL), the latter have an overbar (i.e. SIGNAL). Where a signal has two different and mutually exclusive actions, a dual name is used (e.g. COME/GO).
- Internal signals and variable names (e.g. bits in registers) are always documented as active high.
- When the condition indicated by the name of the signal or variable is true, the signal or variable is said to be true, asserted or to have the value 1.
- When the condition indicated by the name of the signal or variable is not true, the signal or variable is said to be false, de-asserted or to have the value 0.
- When an active high signal is true or asserted, the logic voltage level is high.
- When an active low signal is true or asserted, the logic voltage level is low.
- When an internal signal or variable is set, it has the value 1. A bit is never "set to 0", but "reset to 0".
- When an internal signal or variable is reset, it has the value 0.
- Hexadecimal numbers are indicated by appending an "h", e.g. A70h.

III.4 - Specification

Bitstreams Accepted

MPEG-1 video elementary stream (ISO/IEC 11172-2). CCITT H.261 CIF and QCIF (after unframing and error correction).

Performance

Real-time decoding and display of SIF/525, SIF/625 and CIF pictures at compressed data rates up to 5 Mbit/s. Other combinations of picture size, decoding rate and display rate can be supported, subject to the bandwidth constraints of the memory interface.

Maximum Picture Size

Width : 4080.
Number of macroblocks : limited by memory size.

Motion Vector Range

MPEG-1 : -1024 to 1034 (full pel), -512 to 511.5 (half pel) horizontal and vertical.
H.261 : -15 to 15 (full pel).

Microcontroller Interface

8/16-bit data port with "DTACK" acknowledge.
Intel or Motorola-style protocols selectable.
Single interrupt request pin, vectored or non-vectored modes can be used.

Compressed Data Input

Either 8/16-bit asynchronous input through microcontroller interface, program or DMA controlled, or, input through dedicated serial port.
Peak input rate : 20 Mbit/s (where 1 Mbit/s = 106 bit/s) through the serial port, 10 Mword/s (where 1 Mword/s = 106 word/s) through the microcontroller interface (in practice, the sustained rate will be constrained by the memory bandwidth required for real-time decoding).

Start Code Detection

Automatic detection of start codes of picture layer and above to enable microcontroller to access header data.

DRAM Interface

External DRAM used for storage of picture buffers and bit buffer.

16-bit data bus. Refresh handled by STi3400.
Configurations supported : 4 Mbits (1 bank), 8 Mbits (2 banks), 12 Mbits (3 banks), 16 Mbits (1 or 4 banks), 32 Mbits (1 bank).

Video Output

There are 4 output modes :

- 24-bit RGB 4:4:4
- 8-bit YC_BC_R 4:2:2
- 16-bit YC_BC_R 4:2:2
- 24-bit YC_BC_R 4:4:4

Maximum pel output rate 27MHz (the maximum usable pel rate will be determined by picture size and decoding rate). External pel clock. Horizontal/vertical synchronization and blanking source selectable to be internal or external. Fully programmable internal video timing generator. Support for 525/60 and 625/50 interlaced displays, as well as other user-defined interlaced or non-interlaced formats. Selectable horizontal up-sampling (doubling) by 8-tap filter. Vertical chroma reconstruction by 2-tap filter including 352-sample delay line.

Decoding Pipeline

Instruction register set up each picture defines pipeline operation. Double-buffered quantization matrices enable loading of new tables concurrently with decoding.

Error Concealment

Automatic concealment of errors detected by VLD and decoding pipeline by macroblock copy.

Primary Clock

50MHz maximum.

Power Dissipation

0.6W maximum.

Package

120 pin PQFP.

IV - MICROCONTROLLER INTERFACE AND COMPRESSED DATA INPUT

IV.1 - General

The STi3400 microcontroller interface is asynchronous and has a 16-bit bidirectional data bus and a 7-bit address bus. The data bus can be configured to be of 8 or 16-bit width and the control signals to operate with either Intel or Motorola-style protocols. The port is used for programmed data transfers between the external microcontroller and the STi3400 registers. It can also be used for the transfer of compressed (coded) data to the STi3400.

Compressed data can be input through the microcontroller interface either under program control or by DMA. In addition, a dedicated serial port, which is independent of the microcontroller port, is available for compressed data input.

IV.2 - Interface Signals

The microcontroller interface is made up of the following signals :

Name	Type	Function
D15 - D0	I/O	Bidirectional Data Port
A6 - A0	I	Address
$\overline{CS}$	I	Chip Select/Strobe
$\overline{DS}$ (RD)	I	Data Strobe (Motorola mode), or Read Strobe (Intel mode)
R/$\overline{W}$ (WR)	I	Read/Write Select (Motorola mode), or Write Strobe (Intel mode)
$\overline{DTACK}$	O	Data Acknowledge
$\overline{IRQ}$	O	Interrupt Request
$\overline{IACK}$	I	Interrupt Acknowledge

In Motorola mode, a read or write cycle is controlled by the signals $\overline{CS}$ and $\overline{DS}$; a cycle starts when both signals have gone low and ends when either one of them becomes high. The signal R/W defines the direction of the transfer. The acknowledge signal $\overline{DTACK}$ is always generated in response to the start of a read or write cycle. The timing of a Motorola read cycle is shown in Figure 41 and that of a Motorola write cycle is shown in Figure 42. A simplified Motorola-style interface can be constructed by keeping either $\overline{CS}$ or $\overline{DS}$ permanently low, and using $\overline{DS}$ or $\overline{CS}$, respectively, to control the cycle.

In Intel mode, a read cycle is controlled by signals $\overline{CS}$ and $\overline{RD}$; a cycle starts when both signals have gone low and ends when either one of them becomes high. $\overline{WR}$ must be high throughout a read cycle. A write cycle is controlled by signals $\overline{CS}$ and $\overline{WR}$; a cycle starts when both signals are low and ends when either one of them becomes high. $\overline{RD}$ must be high throughout a write cycle. The acknowledge signal $\overline{DTACK}$ is always generated in response to the start of a read or write cycle. The timing of an Intel read cycle is shown in Figure 41 and that of an Intel write cycle is shown in Figure 43. A simplified Intel-style interface can be constructed by holding $\overline{CS}$ permanently low, and using $\overline{RD}$ and $\overline{WR}$ to define the read and write cycles, respectively.

When the interface is configured in 8-bit mode, only bits D7-D0 of the data bus are used. In 16-bit mode, the address bit A0 must be held at 0.

STi3400 interrupt requests are signalled by $\overline{IRQ}$. This can either be acknowledged with $\overline{DS}$ or the $\overline{IACK}$. In the latter case, a user-defined interrupt vector is output on D15-D0. The STi3400 interrupt mechanism is described in Section IV.6, "Interrupts".

The following signals are related to the control of compressed data input :

Name	Type	Function
$\overline{CDREQ}$	O	Compressed Data Request
$\overline{DMAACK}$	I	DMA Acknowledge
$\overline{DMAREQ}$	O	DMA Request
SD	I	Serial Port Data
SC	I	Serial Port Clock

The signal $\overline{CDREQ}$ becomes high when the compressed data FIFO is full ; no further data must be input until it becomes low again.

When compressed data is input through the data port, D15-D0 (or D7-D0 in 8-bit mode), by DMA, the DMA handshake signals $\overline{DMAACK}$ and $\overline{DMAREQ}$ are used. The STi3400 requests DMA input by asserting $\overline{DMAREQ}$. The external DMA controller indicates that new data is ready by asserting $\overline{DMAACK}$ (the naming of these signals is consistent with the assumption that the STi3400 is the master during a DMA transfer). DMA operation is described in Section IV.5.3, "DMA Transfer".

If compressed data is entered serially, the inputs SD and SC are used. Serial port operation is described in Section IV.5.4, "Serial Transfer".

The signals $\overline{DTACK}$, $\overline{IRQ}$ and $\overline{DMAREQ}$ are open-drain outputs. A 1kΩ pull-up resistor is recommended for use on these signals.

IV - MICROCONTROLLER INTERFACE AND COMPRESSED DATA INPUT (continued)

IV.3 - Interface Configuration

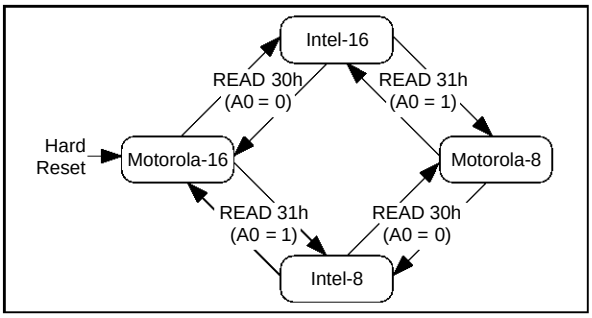
The states in the diagram of Figure 3 represent the four possible configurations of the microcontroller interface. Transferring from one configuration to another is effected by performing reads from the MCF register (addresses 30h and 31h).

After a hard reset, as would be performed after power-up, the interface is in Motorola-16 mode. To change the configuration to Intel-16 mode, a read from address 30h (A6-A0 = 011 0000) must be performed. A further read from address 31h (A6-A0 = 011 0001) changes the configuration to Motorola-8 mode. One more read from address 30h will place the interface in Intel-8 mode. The other transitions possible are shown in Figure 3. This method of setting up the interface configuration is possible because the same read cycle is used in both Motorola and Intel modes (see Figure 41).

Once the desired configuration has been achieved, it can be locked by setting bit MCF.LCK. When the configuration has been locked, the configuration state can be read from the MCF register without causing any further configuration change.

If the STi3400 is to be used in any mode other than Motorola-16, the setting up of the microcontroller interface configuration must be the action after a hard reset.

Figure 3 : Micro Interface Configurations



IV.4 - Register Access

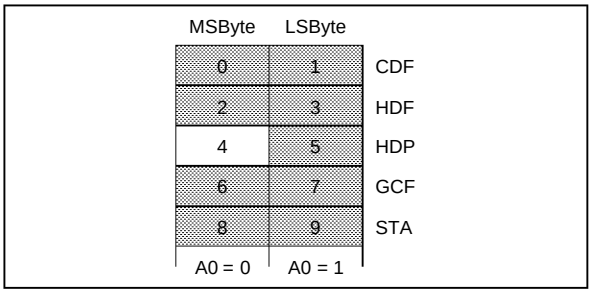
IV.4.1 - Register Addressing

The state of the 6 address bits, A6-A0, defines one of the 64 one-byte internal register locations. The function of each of the registers is detailed in Section XIII, "REGISTERS". Some are read only, some write only, and some read/write.

The internal registers are organised in 16-bit units, as shown in Figure 4. A 16-bit register is mapped into two consecutive addresses. When the microcontroller interface is configured in 8-bit mode, two cycles are required for the read or write of a 16-bit register. In 16-bit mode, in which an entire 16-bit register is accessed in one cycle, the addresses used are the addresses of the MSBytes, i.e. 0, 2, 4, 6, etc. A0 is thus always 0 in 16-bit mode.

For accesses to all register addresses except CDF (for which byte-swap is possible), in both Intel-16 and Motorola-16 modes, the MSByte is transferred on D15-D8, and the LSByte on D7-D0.

Figure 4 : Register Addressing

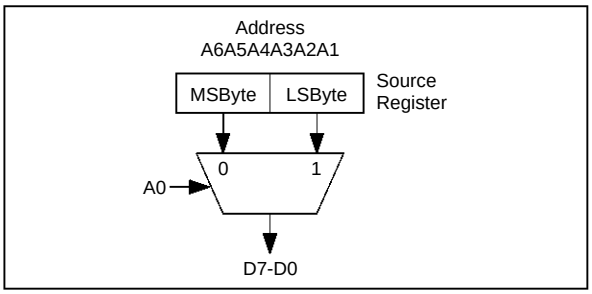


IV.4.2 - Reading in 8-bit Mode

In 8-bit mode, the MSByte of a 16-bit register is addressed with A0 = 0, and the LSByte with A0 = 1. The remainder of the address (A6-A1) defines the word address.

For all registers except HDF, a read of either MSByte or LSByte will cause the register state to be sampled and the appropriate byte, as selected by A0, will be output on D7-D0. This is shown in Figure 5.

Figure 5 : Byte Selection in 8-bit Read



The order in which the bytes are read is unimportant, except :

1. When reading the HDF register, the MSByte must be read first. This operation causes a new word to be extracted from the header FIFO.
2. When reading the ITS register, the MSByte must be read first. The interrupt request is removed when reading the LSByte of the register.
3. Between reading the two bytes of the BBL register, the value of the register could have changed. It is therefore recommended to use a procedure such as that described in the BBL register description in Section XIII.2, "Register Descriptions".

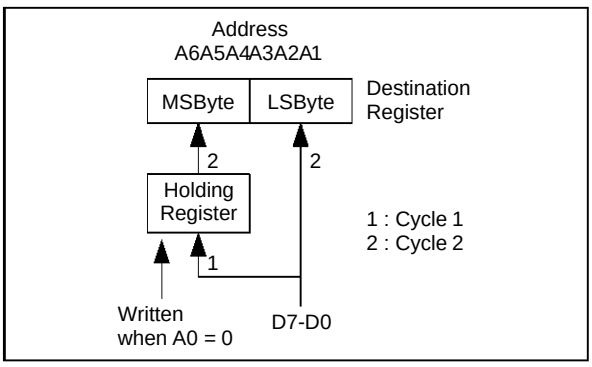
IV - MICROCONTROLLER INTERFACE AND COMPRESSED DATA INPUT (continued)

It is possible to interpose cycles of writes or reads to/from other registers between the two cycles of a read from a register. However this is not recommended, since separating the cycles of read in this way could cause problems of inconsistency if the register state changes between the read cycles.
When it is required to read two consecutive bytes, it is possible to combine these into a single extended cycle. The cycle starts normally with the reading of the first byte. When the assertion of DTACK indicates that the first byte is available, the least significant address bit can be changed. This causes the second byte to be switched to the output. DTACK will remain asserted during the read of the second byte. This type of cycle should not be used for the reading of the ITS register.

IV.4.3 - Writing in 8-bit Mode

This section applies to for writes to all registers except CDF (compressed data FIFO).
In 8-bit mode, the MSByte of a 16-bit register is addressed with A0 = 0, and the LSByte with A0 = 1. The remainder of the address (A6-A1) defines the word address.
To write to a 16-bit register, the most significant byte (A0 = 0) is written first. This byte is stored in an internal holding register during the first cycle and is not written to the destination register, as shown in Figure 6. The state of address bits A6-A1 is not taken into account. In the second cycle, the least significant byte (A0 = 1) is written. In this cycle, both bytes, the new byte and the one stored during the first cycle, are written to the destination register. So for example to write to the GCF register, a write must first be made to address 6, followed by a write to address 7.
It is not possible to write only the LSByte to a register unless it is required to write to the MSByte the same value that was loaded to the last-written MSByte. It is never possible to write only the MSByte.

Figure 6 : Register Write in 8-bit Mode



The two parts of a register write operation must never be interrupted by another register write operation, since the contents of the internal register could be overwritten before it is used. However, writes to a register and CDF can be interleaved, since a separate holding register is used for the latter.

IV.4.4 - Reading and Writing in 16-bit Mode

When operating in 16-bit mode, the least significant address bit (A0) must be fixed at 0.

IV.5 - Compressed Data Input
IV.5.1 - General

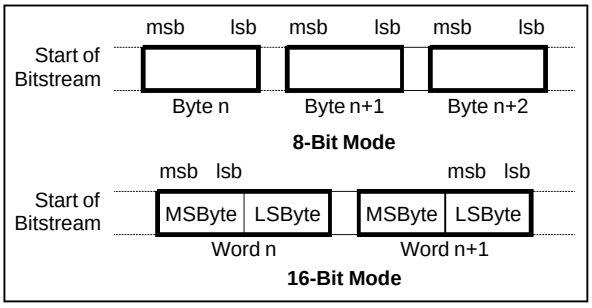
The compressed data input to the STi3400 must be either an MPEG video elementary stream, or an H.261 stream after unframing and error correction. Compressed data input bytes are written into the 512-bit Compressed Data (CD) FIFO (see Figure 1). Data from this FIFO are transferred in 256-bit packets into the bit buffer area of the external memory. The rate at which these burst transfers can occur is governed by the number of higher priority requests waiting for service from the memory controller. The assertion of the signal CDREQ indicates that there is space for at least 2 more bytes in the CD FIFO. Compressed data must never be written when CDREQ is not asserted, since data will be lost.

There are three ways of inputting compressed data :

1. Programmed transfer of bytes or words.
2. DMA transfer of bytes or words.
3. Serial bitstream transfer through the serial port.

For the first two input modes, the compressed data bits are stored in the order most significant bit to least significant bit of the incoming bytes, as shown in Figure 7. The format and ordering of the words in the lower part of the also defines the data storage format in the bit buffer area of the external memory. The MPEG standard requires that start codes in the bitstream be byte-aligned.

Figure 7 : Bitstream Byte and Word Order



IV - MICROCONTROLLER INTERFACE AND COMPRESSED DATA INPUT (continued)

IV.5.2 - Programmed Transfer

Compressed data can be written in the same manner as other register data by writing to CDF in either 8 or 16-bit mode.

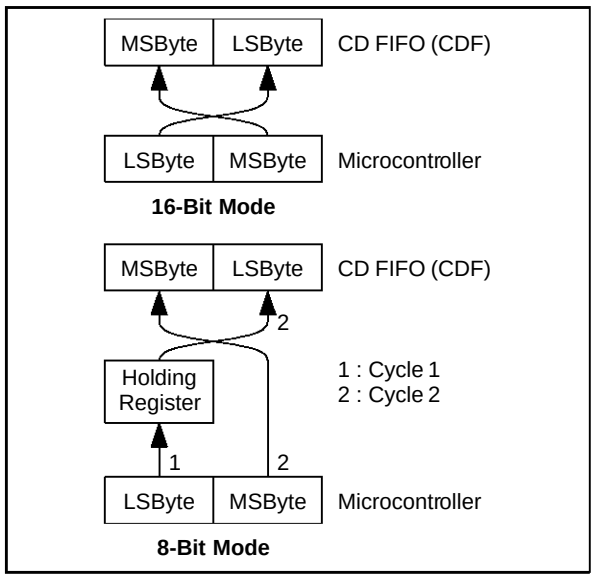
For writing to CDF, byte swap (i.e. Intel, or "little-endian" byte ordering) can be selected by setting bit GCF.BSW. When this mode is enabled, the MSByte and LSByte are exchanged internally before being transferred into the CD FIFO. (This switch occurs after the second cycle when in 8-bit mode). The byte swap mechanism is illustrated in Figure 8.

Byte swap is not possible with any other register.

In 8-bit mode, compressed data write cycles can be combined in any sequence with any other register read/write cycles. The interleaving of write cycles is possible because the CD FIFO has an independent holding register (see Figure 6).

There is a second way of writing to the CD FIFO when the interface is in 8-bit mode, in which A0 must always be 0. This method is described in Section IV.5.3, "DMA Transfer".

Figure 8 : Byte Swap when Writing to CDF



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IV.5.3 - DMA Transfer

The three signals, $\overline{\text{DMAACK}}$, $\overline{\text{DMAREQ}}$ and CDREQ can be used to control DMA transfers into the compressed data buffer. $\overline{\text{DMAACK}}$ and $\overline{\text{DMAREQ}}$ provide an asynchronous handshake for each data transfer, as shown in the timing diagram of Figure 47. Transfers are of bytes or words (with or without byte swap, as defined by the state of bit GCF.BSW), depending on the configuration of the microcontroller interface. If the CD FIFO becomes full after a transfer, $\overline{\text{DMAREQ}}$ remains high and CDREQ becomes high. These signals return to the low (asserted) state when a word has been released from the CD FIFO.

DMA is enabled by setting bit GCF.DMA. This enables the operation of the $\overline{\text{DMAACK}}$ pin.

During a DMA transfer, there are no constraints on the state of the address inputs, A6-A0. If the microcontroller interface is in Intel mode, $\overline{\text{CS}}$ or ($\overline{\text{RD}}$.$\overline{\text{WR}}$) must be high. If it is in Motorola mode, $\overline{\text{CS}}$ or $\overline{\text{DS}}$ must be high.

When the microcontroller interface is configured in 8-bit mode, the first byte written after a hard or a soft reset is stored in the CD FIFO holding register (see bottom of Figure 8). On the next byte transfer, a 16-bit word is written to the CD FIFO. The following byte written is stored in the holding register, and so on. If the writing process is interrupted between the writing of the two bytes of a word, writing will resume correctly after the break. This transfer mode can also be used for non-DMA transfers if A6-A1 = 0, and A0 is held at 0.

Bit MCF.LBT indicates whether the last byte written was transferred to the CD FIFO. When the end of the compressed data stream is reached, if this bit is not set, then an extra byte must be written to CDF in order to flush the last DMA byte into the CD FIFO.

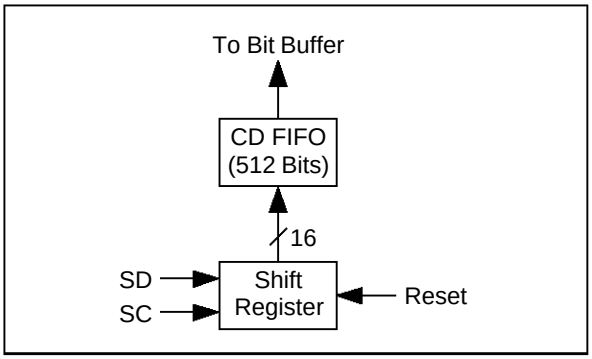
When using DMA, bit CTL.PBO should be set (see Section VII.1, "Bit Buffer Level Control").

IV.5.4 - Serial Transfer

When bit GCF.SER is set, compressed data must be input through the serial port.

This bitstream is transfered through the serial input pin SD. New data is sampled on the rising edge of the serial clock SC, as shown in the timing diagram of Figure 48. When 16 bits of data have been clocked in, they are loaded into the compressed data FIFO. The serial input mechanism is illustrated in Figure 9.

Figure 9 : Serial Input to CD FIFO



3400-10.EPS

IV - MICROCONTROLLER INTERFACE AND COMPRESSED DATA INPUT (continued)

If after clocking in a bit, $\overline{\text{CDREQ}}$ becomes high, then loading of serial data must stop if after 16 SC cycles $\overline{\text{CDREQ}}$ is still high.

The shift register, which performs the serial to parallel conversion, is reset after a hard or a soft reset, and whenever the serial port is selected by setting bit GCF.SER. The latter feature allows resynchronization of the serial port between bursts.

For MPEG bitstreams, the first bit of a start code loaded after a shift register reset must be byte-aligned; the number of any preceding zero bits must be a multiple of 8.

Byte swapping can be used with serially-input data.

IV.5.5 - Flushing of CD FIFO

If it is required to complete the decoding of a sequence before the arrival of another, any data remaining in the CD FIFO must be flushed into the bit buffer. To ensure that the last packet is sent from the CD FIFO, at the end of the first sequence the user program should write 15 zero words if in 16-bit mode, or 31 zero bytes if in 8-bit mode.

IV.5.6 - CD Transfer Rate

The average rate of compressed data input is one of the decoder performance constraints. It is related to picture size, prediction modes and primary clock frequency, according to the relationships given in Section XI, "PERFORMANCE CALCULATION". This rate can be exceeded momentarily though, provided that the number of bits written during a picture period does not exceed the number used in the performance calculation.

For CIF/SIF applications, data can be input continuously at a rate equal to the average rate, without handshake, provided that this does not exceed $0.7 \times f_{primary}$, where $f_{primary}$ is the primary clock frequency. For example, if fprimary is 50MHz, then the maximum continuous input rate is 0.7 x 50 = 35 Mbit/s.

For rates which are momentarily higher than the higher than the average, or for applications with higher than usual display bandwidth requirements, such as 4X resolution still picture display, the signal $\overline{\text{CDREQ}}$ should be continuously monitored.

The CD FIFO can be filled in burst mode at the maximum rate of the microcontroller interface. This is approximately 80 Mbit/s set in 8-bit mode or 160 Mbit/s in 16-bit mode.

IV.6 - Interrupts

The conditions which can cause an interrupt are represented by the bits of the STA register. Any change of state from 0 to 1 of one of these bits (an "event") will cause an interrupt unless it is masked by the corresponding bit of the ITM register being reset. Each event causes a bit of the ITS register to be set, regardless of the state of ITM. Any unmasked bit becoming set in the ITS register causes an interrupt request, indicated by the driving of the open-drain signal $\overline{\text{IRQ}}$ into its asserted (low) state.

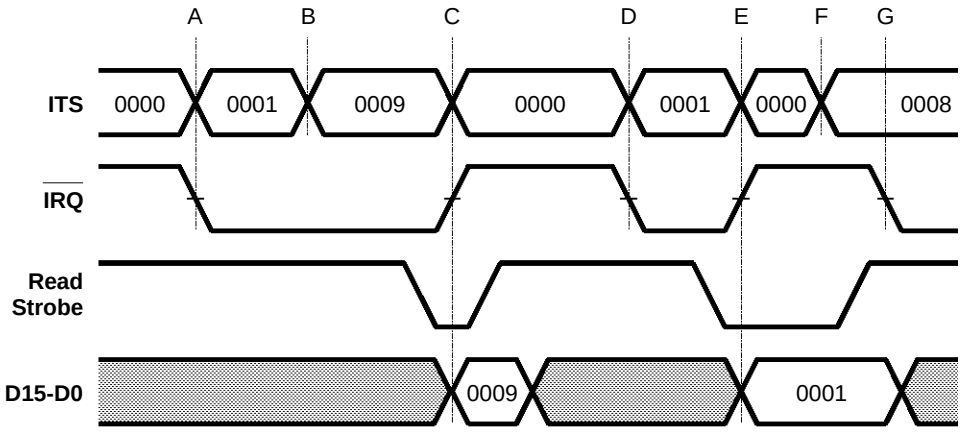
Two modes are available for the handling of the interrupt request: non-vectored and vectored :

- non-vectored interrupt acknowledge : the interrupt is acknowledged and its source(s) identified by reading the ITS register. The reading of this register has the effect of clearing it and thereby removing the interrupt request (i.e. $\overline{\text{IRQ}}$ returns to its undriven (high) state). If the microcontroller interface is in 8-bit mode, the MSByte must be read first. The interrupt request is removed when reading the LSByte. Each byte is cleared as it is read. The timing of the removal of the interrupt request is given in Figure 45. Note that $\overline{\text{IACK}}$ is kept high.
- vectored interrupt acknowledge : the interrupt is acknowledged by asserting the signal $\overline{\text{IACK}}$. In response to this, the value stored in the ITV register is output onto D15-D0 (even when the interface is in 8-bit mode) and $\overline{\text{IRQ}}$ returns to its high state. The timing of the removal of the interrupt request is given in Figure 44. ITS must be read, as explained above, to identify the source(s) of the interrupt.

If, during a read of the MSByte of ITS, an event occurs which affects the LSByte, this will be reflected in the state of the LSByte when it is read. An event affecting the MSByte occurring during the read of this byte, or of the LSByte, will produce an interrupt when the reading of the LSByte is completed. An event occurring during the read of ITS in 16-bit mode will produce an interrupt when the read cycle is completed. The latter case is illustrated in Figure 10.

IV - MICROCONTROLLER INTERFACE AND COMPRESSED DATA INPUT (continued)

Figure 10 : Interrupt Identification



A : STA[0] 0 → 1, $\overline{IRQ}$ asserted
B : STA[3] 0 → 1
C : ITS read, $\overline{IRQ}$ de-asserted
D : STA[0] 0 → 1, $\overline{IRQ}$ asserted
E : ITS read, $\overline{IRQ}$ de-asserted
F : $\overline{STA}$[3] 0 → 1 during read of ITS
G : $\overline{IRQ}$ is asserted at end of read cycle

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V - EXTERNAL MEMORY

V.1 - Memory Interface

The memory interface consists of the following signals :

Name	Function
DD16 - DD0	Bidirectional Data Port
AA9 - AA0	Address
$\overline{RAS3}$ - $\overline{RAS0}$	Row Address Strobes
$\overline{CAS}$	Column Address Strobe
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable

These signals correspond directly the DRAM signals of the same names.

Memories with multiplexed 9-bit row and 9-bit column addresses, or 10-bit row and 10-bit column addresses can be used. The address width is selected by bit GCF.ME9 ; when set the width is 9 bits, when reset 10 bits.

The memory interface is disabled when bit CTL.EDI is reset (the default state). In this state all of the memory interface signals are in their high impedance state. If it is required to keep the $\overline{RAS}$ and $\overline{CAS}$ signals high when the interface is disabled in order to reduce DRAM power consumption, they should be pulled up to V_{DD} with 20kΩ resistors.

DRAM control can be passed to another master by first turning off refresh by setting bit CTL.DRF, and then disabling the interface.

It is recommended that the signals $\overline{RAS3}$ - $\overline{RAS0}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{OE}$ be connected to the memory through 33Ω series resistors.

V.2 - Size and Organization

The maximum amount of memory which can be addressed by the STi3400 is 2^{21} 16-bit words, equivalent to 32 Mbits. Up to 4 banks can be addressed, since 4 RAS signals are provided.

The memory sizes possible are shown in the tables below :

DRAM Type	Memory Organization	Memory Size	Number of Banks
256K x 4, 256K x 16	256K x 16	4 Mbits	1
	512K x 16	8 Mbits	2
	768K x 16	12 Mbits	3
	1M x 16	16 Mbits	4
1M x 4, 1M x 16	1M x 16	16 Mbits	1
	2M x 16	32 Mbits	2

Figure 11 illustrates a typical configuration with a single bank, and Figure 12 shows how two banks are connected.

V - EXTERNAL MEMORY (continued)

Figure 11 : Single Bank Memory Configuration Using 1-Mbit DRAMs

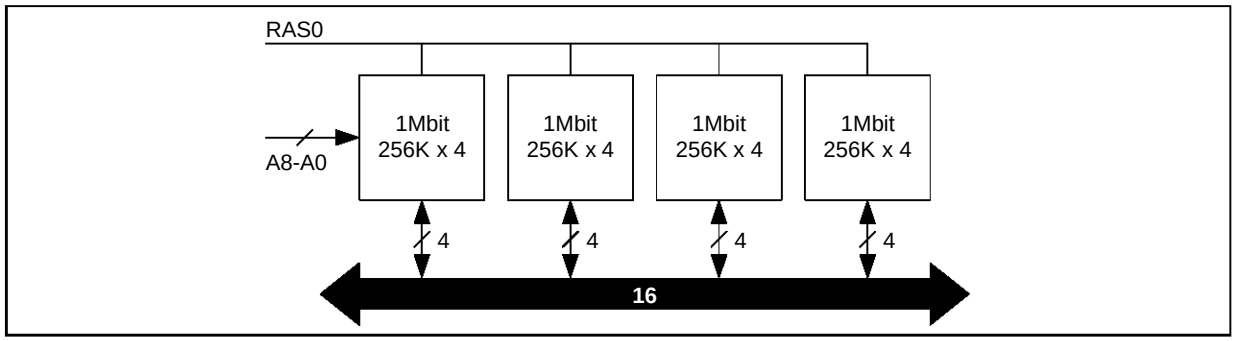


Figure 12 : Maximum Dual Bank Memory Configuration Using 4-Mbit DRAMs

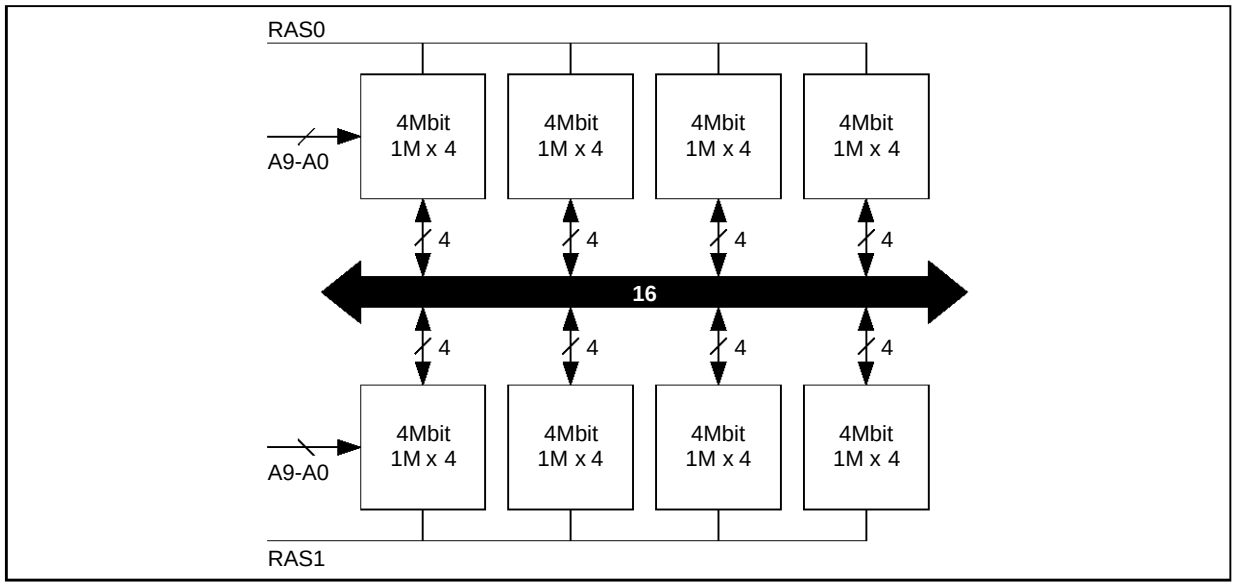
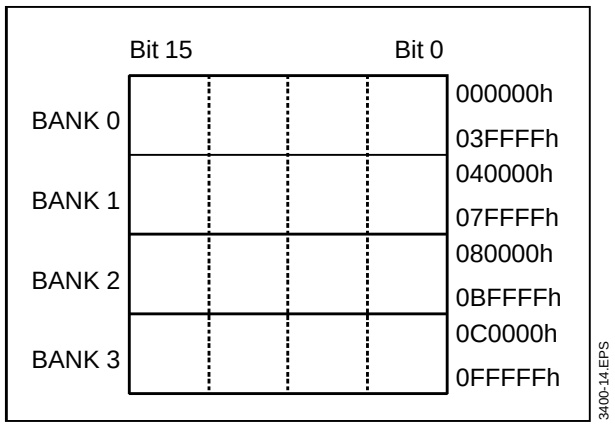
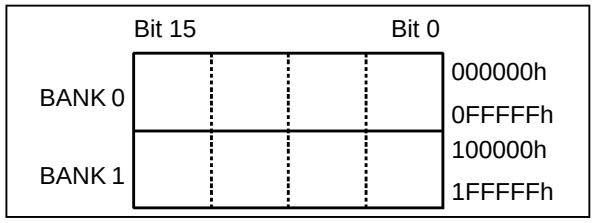


Figure 13 : Address Mapping with 256 kword Memories



When 1 Mword (i.e. those with 10-bit row and column addresses) are used, only 2 banks are available. RAS2 and RAS3 must not be used.
The address mapping when using 256 kword memories is shown in Figure 13, while that when using 1 Mword memories is shown in Figure 14.

Figure 14 : Address Mapping with 1 Mword Memories



V - EXTERNAL MEMORY (continued)

V.3 - Timing Requirements

The timing parameters for the memory interface are given in Section XII.3.2, "DRAM Interface" . In most instances, these are dependant on the primary clock frequency, which could enable slower memories to be used then the primary clock frequency is lower than the maximum. With a primary clock of 50MHz, "-80" or faster memories are required.

The maximum permissible memory access times are related to the memory interface parameters as follows :

$t_{AA} = t_{CAL} - t_{DS}$ (read) = TBD ns
t_{ACP}* = TBD ns
$t_{CAC} = t_{CAS} - t_{DS}$ (read) = TBD ns
$t_{OEA} = t_{OCH} - t_{DS}$ (read) = TBD ns
$t_{RAC} = t_{CSH} - t_{DS}$ (read) = TBD ns

Where T is the primary clock period.
* Also sometimes referred to as t_{CPA}.

V.4 - Refresh

Memory refresh is handled automatically by the STi3400 memory controller by inserting "CAS before RAS" refresh cycles. The duration of a refresh cycle is 9 primary clock periods. During these cycles the RAS signals are driven together, thus refreshing a row from each bank. The refresh period is defined, in units of 3 primary clock periods, by the programming of GCF.RFI[8:0]. For example if 512 memory rows must be refreshed every 8ms and the primary clock is 50MHz, GCF.RFI[8:0] must be loaded with :
8ms/512 x 50MHz/3 = 260 (after rounding down)

V.5 - Memory Mapping Examples

The first example (Figure 15) shows the memory map in a CIF or SIF-625 application in which the picture size is 352 x 288. With 3 picture buffers each occupying 76,032 (352 x 288 x 12 bits) words (1.16 Mbits), there is sufficient space for a 532 kbit bit buffer. The picture buffer addresses must be constrained to start on 128-word boundaries, as explained in Section V.6, "Picture Storage Data Structure".
The second example (Figure 16) shows the memory map in an SIF-525 application in which the picture size is 352 x 240. With 3 picture buffers each occupying 0.97 Mbits (352 x 240 x 12 bits) there is sufficient space for a 1.1 Mbit bit buffer. The picture buffer addresses are constrained to start on 128-word boundaries.

V.6 - Picture Storage Data Structure

Figure 17 shows how the data for a picture is mapped into memory.

Figure 15 : 352 x 288 pictures in 4 Mbits

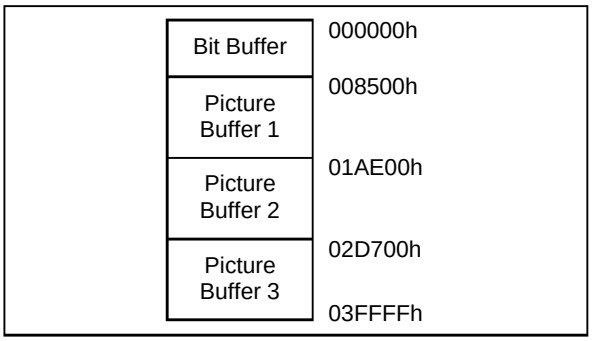


Figure 16 : 352 x 240 Pictures in 4 Mbits

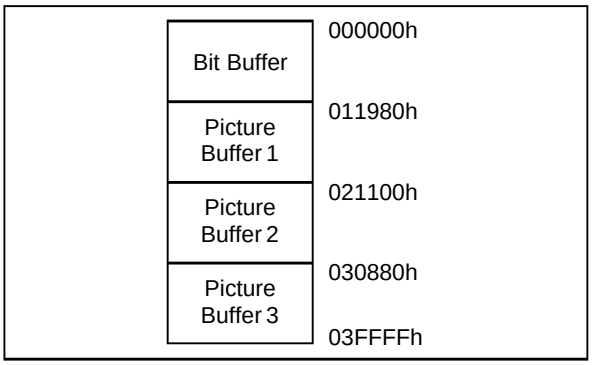
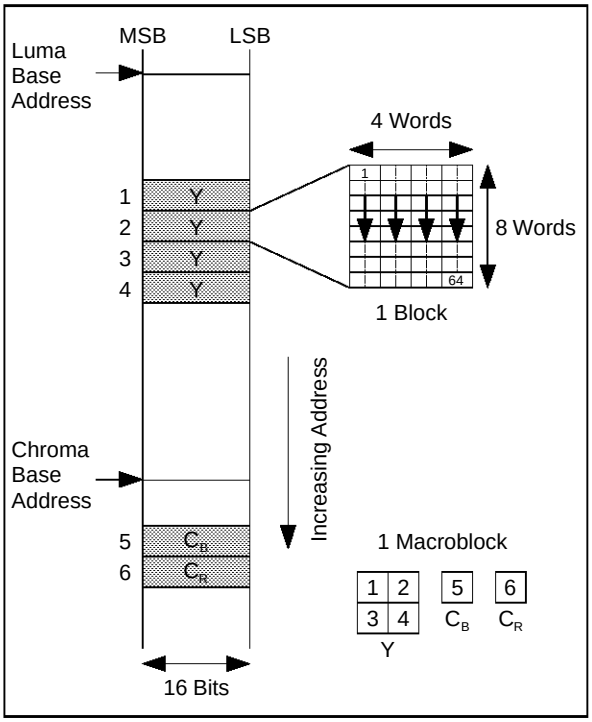


Figure 17 : Storage of a Macroblock



Each 8 x 8 block is stored in 4 vertical stripes of 8 words, requiring a total of 32 words.

V - EXTERNAL MEMORY (continued)

The luminance and chrominance data in each picture buffer are stored separately; first all of the luminance macroblocks, and then all of the chrominance macroblocks. A new macroblock starts every 4 x 32 = 128 words in the luminance areas and every 64 words in the chrominance areas.
The base address of the luminance is defined by the picture buffer base address as set up in one the registers DFP (displayed picture pointer), RFP (reconstructed picture pointer), FFP (forward picture pointer) or BFP (backward picture pointer). The chrominance base addresses are calculated internally using the contents of the DFS (decoded picture size) register.

For example for the display buffer the luminance start address is : 128 x DFP,
and the chrominance start address is :
128 x (DFP + DFS).

The size of the chrominance area is half that of the luminance area.
One memory page contains 512 or 1024 16-bit words, depending on the memory type. One block requires 32 words.
Thus one page can hold the luminance blocks of 4 or 8 macroblocks or the chrominance blocks of 8 or 16 macroblocks. In order to maximise the efficiency of memory access, macroblocks do not cross page boundaries.

V.7 - Memory Test Procedure

The following procedure can be used to test the external memory :

1. Apply a hard reset.
2. Set up refresh period (GCF.RFI[8:0]), set up address bus width (GCF.ME9), enable DRAM interface (CTL.EDI ← 1). Set BBS to be equal to the size of the installed memory. Do not enable decoding (maintain CTL.EDC = 0).
3. Fill the memory with test data by writing to CDF or by clocking it in through the serial port (set GCF.SER appropriately).
4. The test data following it can then be read from HDF. The STA.HFF bit can be polled to determine the status of the header FIFO. (All of the test data can be read directly from the header data since the start code detector (SCD) is inactive after the reset).

VI - RESETS AND POWER-DOWN MODE

VI.1 - Resets

There are three types of reset :
- A hard reset is generated by asserting pin $\overline{\text{RESET}}$ for a duration of at least 10 primary clock cycles.
- A soft reset is generated by setting and resetting bit CTL.SRS. It must be set for a duration of at least 32 primary clock cycles.
- A pipeline reset is generated by setting and resetting bit CTL.PRS.

After a hard reset :
- All decoding and display activity stops.
- All data remaining in the external memory is lost. Any data remaining in the bit buffer, the compressed data FIFO and the header (start code detector) FIFO are lost. BBL is reset.
- The SCD becomes idle.
- The registers are forced into the reset states defined in Section XIII.2, "Register Descriptions".
- The circuit is put into low power mode (defined in Section VI.2, "Power-Down Mode"), with the video and memory interfaces placed into a high impedance state.
- The video timing generator (VTG) is disabled, and the video synchronization I/Os are put into input mode.
- The microcontroller interface is placed in Motorola 16-bit mode.
- The interrupt unit is reset.
- The serial input shift register is reset.

A hard reset would normally be used after power-up and when it is required to place the circuit in low power mode.

After a soft reset :
- All processes concerning decoding and bit buffer control are reset. Any data remaining in the bit buffer, the compressed data FIFO and the header FIFO are lost. BBL is reset.
- The SCD becomes idle.
- Bit MCF.LBT is reset.
- All other registers maintain their contents and the display process is not disturbed.
- The serial input shift register is reset.

A soft reset would normally be used when the decoding of the current bitstream must be terminated for any reason.
After a hard or a soft reset, the first task performed by the pipeline when it has been enabled will always be a search for the next start code. The bit buffer data is flushed until the start code is detected by the pipeline.
A pipeline reset terminates the decoding of the current picture. The remaining bits of the picture are flushed from the bit buffer until the next picture start code is detected by the pipeline. At this point normal behaviour is resumed, i.e. the pipeline waits for the next picture decoding instruction. No other part of the circuit is affected by a pipeline reset. A pipeline reset would normally be used as part of a manual error recovery procedure.

VI - RESETS AND POWER-DOWN MODE (continued)

VI.2 - Power-Down Mode

Low power mode is entered after a hard reset, or by resetting bits CTL.EVI, CTL.EDI and CTL.ECK. In low power mode the video and memory interfaces are disabled. In low power mode, the registers do not lose their contents (if there was no hard reset) and can be accessed normally. All data stored in the external memory is lost. If the external clocks, CLK and PIXCLK, are disabled, power dissipation in this mode is the minimum possible.

VII - BIT BUFFER AND START CODE DETECTION

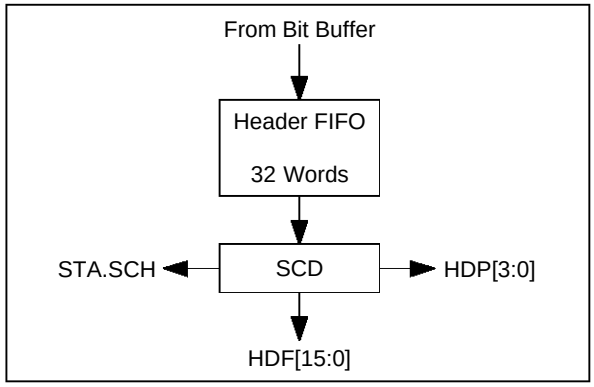
VII.1 - Bit Buffer Level Control

The mechanism of writing compressed data into the bit buffer through the CD FIFO is detailed in Section IV.5, "Compressed Data Input".
As part of the initialization sequence of the decoder, the registers BBS (bit buffer size), BBB (threshold for generation of BBE interrupt), and BBT (threshold for generation of BBF interrupt) must be set up. The bit buffer starting address is always 000000h. The amount of data in the bit buffer is available at any time (in units of 2 kbits) by reading the BBL register. When this level is greater than the value loaded into the BBT register (also defined in units of 2 kbytes), the status bit STA.BBF becomes true. This can be used to generate a "bit buffer nearly full" interrupt. When the bit buffer level is lower that defined in the BBB register, the status bit STA.BBE becomes true. This can be used to generate a "bit buffer nearly empty" interrupt.
When the CD FIFO is full, the status bit STA.BFF is true. This bit is thus equivalent to the signal CDREQ.
If the bit CTL.PBO is set, then transfer of data from the CD FIFO to the bit buffer is prevented if the bit buffer level is at or above the level defined in the BBT register. If BBT is set to a value equal to the top of the bit buffer, then this automatic mechanism will ensure than overflow never occurs. If the bit CTL.PBO is set, then BBT defines a "full" rather than "nearly full" level and should be set equal to BBS to optimize memory usage.

VII.2 - Start Code Detection

The start code detector (SCD) operates in parallel with the decoding pipeline. The purpose of this unit is to give external access to the header data which follows start codes in the input bitstream.
Compressed data is read twice from the bit buffer - once into the pipeline, and once into the SCD through the 32-word header FIFO. The transfer of data into the header FIFO does not affect the bit buffer level; only the data transfer into the decoding pipeline can reduce this. The relationship of the header FIFO and start code detector is shown in Figure 18. Data is extracted from the header FIFO either by the user reading from the HDF register location, or by the SCD itself when start code detection is in progress. In the latter case, the bitstream data is flushed through the SCD and discarded.

Figure 18 : Start Code Detector and Header FIFO



Automatic start code detection stops when a start code is found by the SCD. This event can be signalled by the interrupt associated with STA.SCH. The start code can be read and the data following it, usually header data, can then be read manually from the HDF register location. Automatic start code detection is initiated in two ways :

- Whenever the internal event DSYNC occurs. DSYNC is derived from VSYNC as described in Section VIII.4, "Decoding Task Control". A DSYNC is generated every time the pipeline starts a new picture decoding task.
- Manually by writing to the HDS register location.

After a hard or soft reset, the SCD is idle. The header FIFO will be filled automatically from the bit buffer as soon as data is available. This data can be extracted by reading from the HDF register location. As soon as 16 words have been freed in the header FIFO, another packet of data will be transferred from the bit buffer. If a start code is recognised by the SCD during the reading, the status bit STA.SCH will still become set, even though automatic start code detection is not enabled.

The status bits STA.HFF (header FIFO full) and STA.HFE (header FIFO empty) can be used to control the header FIFO reading process. STA.HFF is 1 when there are at least 16 words of data available in the header FIFO.

VII - BIT BUFFER AND START CODE DETECTION (continued)

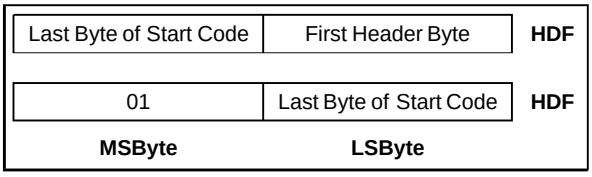
MPEG Mode

If the STi3400 is in MPEG mode, the SCD detects all start codes other than slice start codes; all patterns "000001XXh", where "XX" has values other than 01h through AFh, occurring in the bitstream are detected.

After detection of a start code the HDF register will be one of the states shown in Figure 19.

The first step is to examine the MSbyte of HDF. If this contains "01", then the start code can be identified by reading the LSByte, which will contain the last bye of the start code "XXh". If the first byte is not "01" then it must be the last byte of the start code, "XXh", and the second byte is the first byte of the header data. In both cases subsequent reads from HDF will give access to the header data which follows the start code, where the data is ordered as shown in Figure 7. An alternative method of determining alignment is to read the HDP register. A returned value of 0 corresponds to the upper situation of Figure 19 ; a value of 8 corresponds to the lower situation.

Figure 19 : States of HDF after Start Code Detection



H.261 Mode

If the STi3400 is in H.261 mode, only picture start codes, "00010h", are detected. Since start codes are not byte-aligned in H.261 bitstreams, when the SCD stops on detection of a picture start code, the start code could be in any position in HDF. It is necessary to read HDP determine the alignment. The value returned give the bit position, counting from left to right, in the HDP register of the first bit following the start code "00010h". For example if 0 is read from HDP, the whole of HDF contains header data, while if 15 is read, then only one bit of header data is available in bit HDF[0].

Scanning for start codes will recommence on the next DSYNC or write to HDS. Whenever a start code has been detected, the HDF register must be read in order for the start code detector to restart correctly.

In continuous operation the start code detection and reading of header data will always be one picture in advance of the decoding process. The microcontroller therefore has almost an entire picture period in which to analyse the headers and make the appropriate decisions. When one or more pictures are to be skipped by the decoding pipeline the microcontroller needs access to more than one picture header in a decoding period (the period between two DSYNCs). This is made possible by restarting start code searches by writing to HDS.

More information on STi3400 control and the use of the SCD is given in Section X, "CONTROL OF THE STi3400".

VII.3 - Tracking of Time-Stamps

A mechanism is provided to enable the association of the time-stamps which are included in video packet headers with the times at which particular pictures are decoded. This is needed because the number of pictures which may be stored in the bit buffer at any instant is unknown, and therefore there is a variable delay between the input of a picture into the bit buffer and its entry into the decoding pipeline.

There is a 24-bit counter at the output of the CD FIFO - bit buffer - header FIFO chain, as shown in Figure 20. Each time a 16-bit word is read from the header FIFO the counter BRA is incremented. The counter is modulo 2^{24}, i.e. the state following FFFFFF is 000000. The length of this counter corresponds to approximately 3.7 minutes of bitstream data at a rate of 1.2-Mbit/s. Since this counter is not reset, by either a hard or a soft reset, its initial state must be recorded and subtracted from subsequent count values.

When the first byte of video data from a new packet containing a time-stamp is written into the CD FIFO, the time-stamp and a byte count are stored as an item in a list maintained by the microcontroller. This byte count is updated at the start of every packet by adding the packet length in bytes extracted from the "packet_length" field of the packet header.

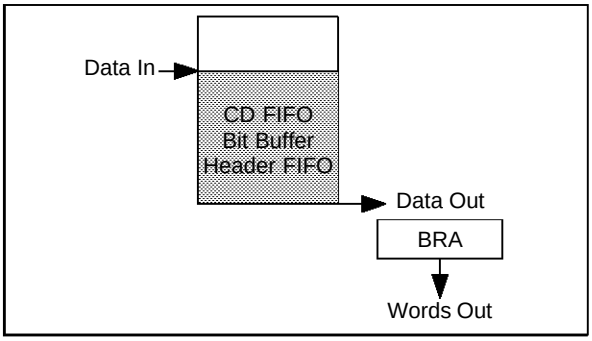
When a picture start code is detected by the start code detector, BRA is read. If this value multiplied by 2 (to give bytes) is greater (modulo 2^{24}) than the last byte count in the list maintained by the microcontroller, then the next picture to be decoded is associated with the time-stamp stored at this position of the list. How this information is used will depend on the synchronization algorithm employed.

In the special case in which slices do not span video packet boundaries, the start code detector can be used to find packet start codes. In this case the time-stamps can be read directly from the header FIFO. However, this method would only be possible if the encoder multiplexer were constrained.

More information on the handling of synchronization is given in Section X.5, "A/V Sync".

VII - BIT BUFFER AND START CODE DETECTION (continued)

Figure 20 : Bit Buffer Read Counter



VIII - DECODING PIPELINE

VIII.1 - General

The pipeline is that part of the circuit which converts the compressed bitstream data for each picture into a decoded (or reconstructed) picture. The operation of the pipeline is controlled picture-by-picture. The decoding of a new picture can potentially start on every VSYNC, but for many applications the rate of decoding is less than the VSYNC rate.

The pipeline is controlled by the pipeline controller (see Figure 1). The pipeline controller starts decoding by issuing a DSYNC signal, which is also sent to the start code detector. When the pipeline has completed its decoding operation, a signal is sent to the pipeline controller, which is then able to launch another decoding operation, either immediately or in synchronism with a VSYNC event.

The pipeline receives its compressed data from the bit buffer. This data is first processed by the variable length decoder (VLD) which regenerates the run/level coded DCT coefficients and the motion vectors (if present) for each macroblock. The picture data is reconstructed by passing the run/level data through the inverse quantizer and inverse DCT blocks. For non-intra macroblocks this is then added to the predictors which have been fetched from the memory according to the macroblock prediction modes and motion vectors. In the case of interpolated predictors, a forward and a backward predictor macroblock are fetched and averaged before the addition. In H.261 pictures, predictors may be filtered. For skipped macroblocks the VLD generates blocks containing zero data. Finally, the decoded picture is written back into the memory, from where it can be accessed by the display unit for output.

In order to bypass the header bits in the data stream which are not used by the pipeline, there is a start code detector at the input to the pipeline. This is able to bypass all bits until a slice start code is found. From this point on all of the coded data is sent to the VLD for decoding. Picture start codes are also recognised, since the detection of the start code of the following picture is the condition which is used to terminate the decoding of a picture.

The pipeline needs to skip through picture data for various reasons. The different possibilities are :

- Skip to Next Picture. This occurs either after a pipeline reset (see Section VI.1, ”Resets”), or when the decoding instruction specifies that 1, 2 or 3 pictures should be skipped (see Section VIII.4, ”Decoding Task Control”). Compressed data is skipped until the next picture start code (or next but 1 or 2) is found, after which the pipeline indicates task completion and waits for a new instruction.
- Skip to Next Slice. This occurs after a soft reset (see Section VI.1, ”Resets”) or error concealment (see Section VIII.6, ”Error Recovery and Missing Macroblock Concealment”). Compressed data is skipped until the next slice start code in the picture is found, after which normal decoding resumes.

Before starting to decode a sequence, certain static parameters must be set up. These are :

- MPEG or H.261 mode selection. Bit GCF.H261 must be reset for an MPEG sequence, set for an H.261 sequence. If in H.261 mode, bit GCF.CIF must be set if the picture format is QCIF.
- Decoded picture size. Register DFW must be set up with the picture width in macroblocks, and register DFS must be set up with the number of macroblocks in the picture.

Decoding is enabled by setting bit CTL.EDC. DSYNCs will only be generated when this bit is set.

VIII.2 - Quantization Table Loading

The two quantization matrices (intra and non-intra) used by the inverse quantizer in MPEG mode must be initialized by the user. There are no built-in quantization matrices. Therefore, they must be loaded either with default matrices or with those extracted from the bitstream by the microcontroller. The quantization tables are double-buffered. This enables one or both tables to be updated without disturbing the decoding task in progress. The STi3400 maintains two bits which record whether one or both of the tables have been modified. A modified table is brought into operation at the start of the next decoding task, i.e. when the next DSYNC occurs, if the bit INS.QMS is set. After a table has been swapped in this way, it cannot be swapped again until a new table has been written.

VIII - DECODING PIPELINE (continued)

After a hard reset, the same pair of tables is always selected. Any data previously loaded into the tables is not affected. Other types of reset have no effect on the quantization table contents or selection.

The quantization tables are written at address QMW. The commands QMN and QMI are used to control access to the tables. The writing procedure is described below.

Intra Table Loading Procedure

The intra table must first be initialized for writing by sending command QMI. The table data are then transferred sequentially by writing 32 words to the QMW register address, the order of data being the same as that used in the MPEG bitstream, i.e. in zig-zag order.

Non-Intra Table Loading Procedure

The non-intra table must first be initialized for writing by sending command QMN. The table data are then transferred sequentially by writing 32 words to the QMW register address, the order of data being the same as that used in the MPEG bitstream, i.e. in zig-zag order.

VIII.3 - Picture Pointers

Before the decoding of each picture the following picture buffer pointers must be set up :
RFP - Reconstructed Picture Pointer
FFP - Forward Prediction Picture Pointer
BFP - Backward Prediction Picture Pointer

(A fourth pointer, DFP, the displayed picture pointer is described in Section IX.3, "Setting up the Display").

RFP defines the memory buffer to which the decoded picture is written. FFP and BFP define the areas in memory from which the predictors are fetched.

VIII.4 - Decoding Task Control

A task is a single picture decoding operation. A task is specified by the task descriptor or instruction, which is set up before the decoding of each picture. A task commences when the internal signal DSYNC is generated. A task completes (the pipeline becomes idle) when the picture header of the following picture is detected by the pipeline. The instruction is double buffered, so that during execution of a decoding task, the instruction for the next task can be set up by the microcontroller. When the next instruction is activated, a DSYNC can be generated, and the next decoding task executed. The buffering mechanism is illustrated in Figure 21.

The Instruction is written into the INS register. If a new instruction is not written, the new task descriptor will be the same as the previous one.

Normally, it is a VSYNC that starts the execution of a new instruction, and the succeeding generation of DSYNC. If however, a VSYNC occurs before task completion (i.e. before the pipeline becomes idle), the start of the next task will be delayed until the present one is completed. In this way the decoding of a picture can be allowed to extend beyond the nominal period allotted to it, one or two VSYNC periods.

Two status bits are associated with pipeline task execution. STA.PSD indicates the occurrence of a DSYNC. STA.PID indicates that the pipeline is idle.

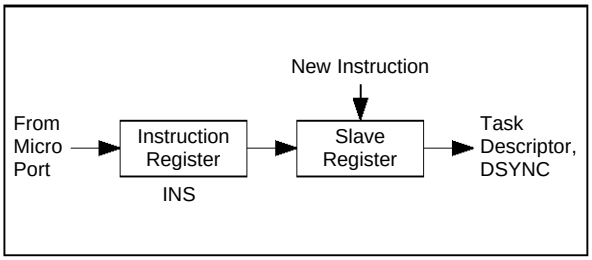
The operation of the pipeline controller is shown in the state diagram of Figure 22.

The instruction bits which affect state transitions are INS.WAIT, INS.RPT and INS1.SKP[1,0]. The events which can cause the execution of a new instruction are VSYNC and CTL.FIN (user-initiated task execution). IDLE and END OF SKIPPING indicate the state of the pipeline.

The resting state of the controller is "task complete" which is entered after all resets (hard, soft or pipeline) and when a decoding task or skipping is completed. If a VSYNC or user-initiated execution request occurs while the controller is in this state, the controller moves to state "new instruction". Here the new instruction is loaded using the mechanism shown in Figure 21.

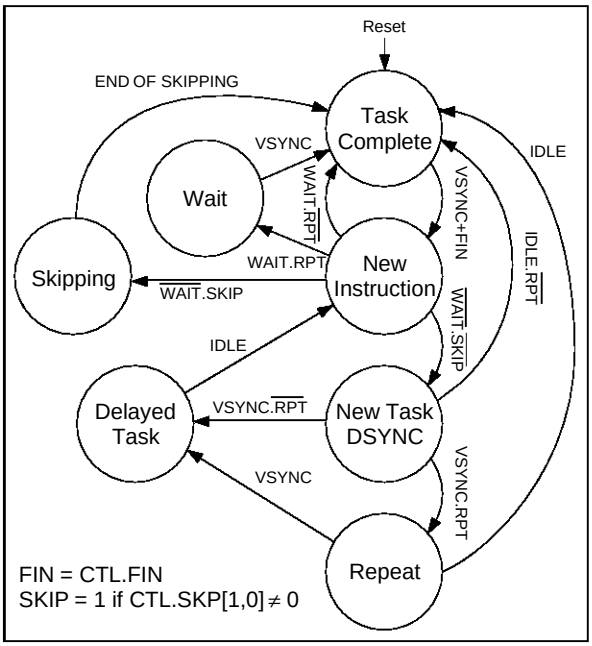
If the action required is "wait for one VSYNC period", i.e. do not generate a DSYNC and thus not start the pipeline and start code detector, bit INS.WAIT must be set and bit INS.RPT must be reset. The controller returns to state "task complete" and waits for the next VSYNC. If the action required is "wait for two VSYNC periods", the both bit INS.WAIT and INS.RPT must be set. The controller now passes through the states "new instruction" and "wait".

Figure 21 : Instruction Buffering



VIII - DECODING PIPELINE (continued)

Figure 22 : Task Control State Diagram



If it required to skip 1, 2 or 3 pictures, then bits INS.SKP[1,0] will be set to a non-zero value. In this case, on execution of the new instruction, the controller will enter state "skipping" (without generation of DSYNC) while the pipeline is performing the picture skipping operation. When skipping is complete, the pipeline asserts END OF SKIPPING, and control returns to state "task complete". Note that INS.WAIT takes priority over INS.SKP[1,0] ; if both are defined, then no picture skipping will occur. If it is required to start decoding the following picture immediately after skipping, or to perform further picture skips before the next VSYNC, user-initiated instruction execution is necessary using bit CTL.FIN.

If the pipeline and start code detector are to be started, then bit INS.WAIT must be reset. The will cause the controller to enter the state "new task" at which time a DSYNC is generated. The pipeline will now execute a picture decoding operation.

If the time allocated to the task is one VSYNC period, INS.RPT must be reset. The controller will remain in state new task" until either the task completes or a VSYNC occurs. In the former case, the controller returns to state "task complete" and waits for the next VSYNC. In the latter case, the task has overrun and VSYNC arrives before IDLE. The state "delayed task" is entered. The controller remains here until IDLE occurs, when the state "new instruction" is immediately entered. Thus the next task is chained immediately to the one just completed.

If the time allocated to the task is two VSYNC periods, INS.RPT must be set. The controller will remain in state "new task" until the VSYNC at the end of the first period occurs. It now moves into state "repeat". The controller will remain in this state until either the task completes or the second VSYNC occurs. In the former case, the controller returns to state "task complete" and waits for the next VSYNC. In the latter case, the task has overrun and VSYNC arrives before IDLE. The state "delayed task" is entered. The controller remains here until IDLE occurs, when the state "new instruction" is immediately entered. Thus the next task is chained immediately to the one just completed.

VIII.5 - Decoding Task Specification

The decoding task to be performed by the pipeline is specified by the remaining bits of the instruction.

The picture coding type, equal to the two least significant bits of the picture_coding_type field of the MPEG picture header, is programmed into bits INS.PT[1,0]. In H.261 mode, the picture type is always P, i.e. INS.PT[1,0] = 2.

The forward motion vector range and type are programmed into bits INS.FF[3:0]. This field does not have to be set up when decoding an MPEG I-Picture. INS.FF[3] is equal to the full_pel_forward_vector bit of the MPEG picture header. It is set to 1 in H.261 mode. INS.FF[2:0] is equal to the forward_f_code of the MPEG picture header. It is set to the value 1 in H.261 mode.

The backward motion vector range and type are programmed into bits INS.BF[3:0]. The field only needs to be set up when decoding an MPEG B-Picture. INS.BF[3] is equal to the full_pel_backward_vector bit of the MPEG picture header. INS.BF[2:0] is equal to the backward_f_code of the MPEG picture header.

The bit INS.OVW must be set when the picture is being reconstructed into the same buffer as that from which the displayed picture is being read, i.e. RFP = DFP. Overwrite mode is explained in more detail in Section X.3, "Use of Picture Buffers".

VIII - DECODING PIPELINE (continued)

VIII.6 - Error Recovery and Missing Macroblock Concealment

There are three types of error which can be detected by the STi3400 while decoding a picture :

1. VLD Error. This occurs when the VLD detects a syntactical or semantic error in the incoming bit-stream. A VLD error is flagged by status bit STA.VER becoming set.
2. Pipeline Error. This occurs when, due to a bitstream error which was not detected by the VLD, either more than 64 coefficients are reconstructed in a block or more than 6 blocks are reconstructed in a macroblock. A pipeline error is flagged by status bit STA.PER becoming true.
3. Severe Error. This occurs when the number of macroblocks reconstructed in a picture is greater than the number stored in the DFS register. A severe error is flagged by status bit STA.SER becoming true.

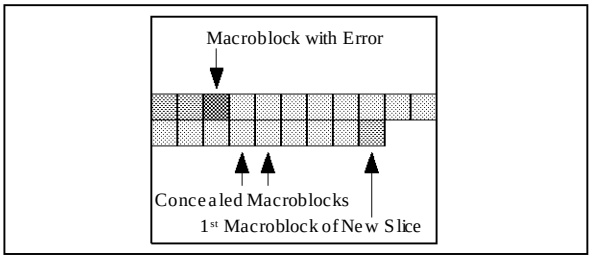
Whenever one of these errors occurs, decoding and reconstruction stops. The interrupts associated with the error status bits should not be masked.

The following recovery options are available :

- ***Automatic Error Concealment on VLD or Pipeline Error :***
  The process of macroblock concealment is illustrated in Figure 23. If a VLD error is detected while decoding a macroblock, error concealment mode can be entered. In this mode the VLD stops decoding and scans the bitstream until the next start code is found. If this code is a slice start or GOB code, the missing macroblocks are replaced with concealment macroblocks and decoding starts again at the new slice/GOB. The macroblock in which the error was found is not concealed. If the next start code found is a picture start code, the missing macroblocks are not concealed and the decoding of the picture terminates (if the picture start code is intact). The missing macroblocks in the displayed picture buffer will contain the data that was already present at the same macroblock positions.
  The concealment macroblocks are obtained from previously reconstructed pictures, using the following rules :
  - P-pictures (and H.261) : the concealment macroblocks are fetched as predictors with a zero vector from the forward reference picture, whose buffer address is defined by FFP.
  - B-pictures : concealment macroblocks are constructed from macroblocks in one or both of the forward and backward reference pictures, using the prediction mode and vector of the last decoded macroblock.

  To enable automatic error concealment on occurrence of an VLD or a pipeline error, bit CTL.EEC must be set.
- ***User-Initiated Error Concealment :***
  The following procedure can be used for the initiation of an error concealment operation under user control. This would not normally be used, since the automatic concealment mechanism achieves the same effect.
  - Enable VLD and pipeline error interrupts
  - If an interrupt occurs :
    Wait until at least 70 primary clock cycles have occurred since the status bit became set,
    Set bit CTL.ERC,
    Wait for at least 100 primary clock cycles,
    Reset bit CTL.ERC.
- ***Automatic Pipeline Reset on VLD or Pipeline Error :***
  If bit CTL.ERP is set, then a pipeline reset will be generated whenever a VLD or a pipeline error occurs. The effect of a pipeline reset is described in Section VI.1, "Resets". If a pipeline reset is generated, the remainder of the picture will not be reconstructed ; the data displayed will be that which was already in the buffer from a previously decoded picture
- ***Automatic Pipeline Reset on Severe Error :***
  If bit CTL.ERS is set, then a pipeline reset will be generated whenever a severe error occurs. The effect of a pipeline reset is described in Section VI.1, "Resets". If a pipeline reset is generated, the remainder of the picture will not be reconstructed; the data displayed will be that which was already in the buffer from a previously decoded picture.
- ***User Initiated Resets :***
  A pipeline reset can be generated by the user as an alternative to the automatic mechanisms described above, or in response to other types of system error after which it is required to abandon the decoding of the present picture.
  A soft reset, whose action is described in Section VI.1, "Resets", is a last-resort action in which decoding of the current sequence is terminated.

Figure 23 : Macroblock Concealment



IX - DISPLAY FUNCTIONS

IX.1 - Functions of the Display Unit

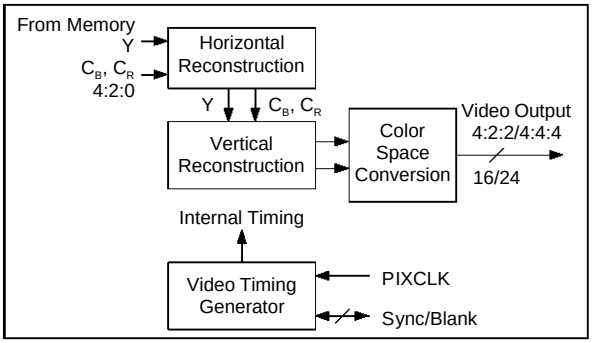
The display unit performs the following functions :

- Requests and receives from the picture buffer in external memory the decoded picture data for display,
- Optionally performs horizontal duplication (with or without filtering) of both luminance and chrominance data,
- Reconstructs vertical data (with or without filtering) to create 4:2:2 sample format,
- Optionally performs colour space conversion for RGB 4:4:4 output.

In addition these is an on-chip video timing generator (VTG) which can be selected as the source of system video timing.

Figure 24 is a simplified block diagram of the display unit, showing the sequence in which the horizontal and vertical sample reconstruction operations occur. The picture data is received from the display frame buffer area of the external memory through the display FIFO into the luma and chroma horizontal reconstruction filter. The lines of a frame can be read out from the memory either in interlaced or progressive order. The horizontal and vertical clipping values set up by the user defines which pel will be the first one of a picture to be read from the FIFO. Horizontal reconstruction is enabled when the length of the displayed lines is twice that of the decoded lines. Two modes are possible, a simple duplication of data, or upsampling of luma and chroma with an 8-tap filter. Vertical reconstruction of chrominance data is performed either by simple duplication of by use of a 2-tap filter which includes a 352-sample delay line.

Figure 24 : Display Unit Block Diagram



IX.2 - Video Interface

IX.2.1 - Pel Output Modes

The following signals (Table below) relate to the output of video data.

In response to each rising edge of PIXCLK a new word of video data is available at the video port.

The timing is given in Section XII.3.5, "Video Interface Timing". Three output modes are available, 24-bit RGB 4:4:4, 16-bit YC_BC_R 4:2:2 and 24-bit YC_BC_R 4:4:4.

Name	Type	Function
RY7-RY0	O	Video Port R or Y or $Y/C_B/C_R$
GC7-GC0	O	Video Port G, C_B
BC7-BC0	O	Video Port B or C_R or C_B/C_R
PIXCLK	I	Pel Clock
$\overline{\text{PIXOE}}$	I	Pel Port Output Enable

Video Output Mode Selection

	DCF.YUV	DCF.V08	XDO.V.24
24-Bit RGB	0	0	1
24-Bit YC_BC_R	1	0	1
16-Bit YC_BC_R	1	0	0
8-Bit YC_BC_R	1	1	0

24-bit RGB 4:4:4

In this output mode the three co-sited colour samples of every pel are output on every cycle of PIXCLK on ports RY7-RY0, GC7-GC0 and BC7-BC0 in the sequence :

RY7-RY0	R^1	R^2	R^3	R^4
GC7-GC0	G^1	G^2	G^3	G^4
BC7-BC0	B^1	B^2	B^3	B^4

8-bit YC_BC_R 4:2:2

In this mode samples are output on Port R/Y/YC_BC_R is the sequence
C_B^1 Y^1 C_R^1 Y^2 C_B^3 Y^3 C_R^3.

In this case, pixel clock must be twice the one in 16/24 bits mode (usually 27MHz).

16-bit YC_BC_R 4:2:2

In this mode the samples are output on ports RY7-RY0 and BC7-BC0 in the sequence :

RY7-RY0	Y^1	Y^2	Y^3	Y^4
BC7-BC0	C_B^1	C_R^1	C_B^3	C_R^3

Y^1, C_B^1 and C_R^1 are the co-sited samples of the first pel, while Y^2 is the luminance only sample of the second pel. The next three refer to the third pel, and so on.

24-bit YC_BC_R 4:4:4

In this mode the samples are output on ports RY7-RY0, GC7-GC0 and BC7-BC0 in the sequence :

RY7-RY0	Y^1	Y^2	Y^3	Y^4
GC7-GC0	C_B^1	C_B^1	C_B^3	C_B^3
BC7-BC0	C_R^1	C_R^1	C_R^3	C_R^3

Y^1, C_B^1 and C_R^1 are the co-sited samples of the first pel, while Y^2 is the luminance only sample of the second pel. The two chrominance output in the second cycle are copies of those output in the first cycle. The next three refer to the third pel, and so on.

When PIXOE is high, RY7-RY0, GC7-GC0 and BC7-BC0 are in their high impedance state.

IX - DISPLAY FUNCTIONS (continued)

IX.2.2 - Video Levels

RGB output is obtained by application of the transform according to CCIR 601 as shown below.

$R = Y + 1.370 \times (C_R - 128)$

$G = Y - 0.698 \times (C_R - 128) - 0.336 \times (C_B - 128)$

$B = Y + 1.730 \times (C_B - 128)$

If Y has a range of 16 to 235, and C_B, C_R are in the range 16 to 240, as defined in CCIR 601, then R,G,B will be in the range 16 to 235.

The output level during blanking periods is selectable with bit DCF.BNK. If this bit is reset, the output level is (R,G,B) = (0,0,0) or (Y,C_B,C_R) = (0,128,128). It this bit is set, the level is (R,G,B) = (16,16,16) or (Y,C_B,C_R) = (16,128,128).

IX.2.3 - Synchronization Signals

The following synchronization and blanking signals are provided :

Name	Type	Function
$\overline{\text{HSYNC}}$	I/O	Horizontal Sync
$\overline{\text{VSYNC}}$	I/O	Vertical Sync (input), or Vertical or Composite Sync (output)
E/$\overline{\text{O}}$	I/O	Even/Odd Field Selection
$\overline{\text{HBLANK}}$	I/O	Composite Blanking (input), or Horizontal Blanking (output)
$\overline{\text{VBLANK}}$	O	Vertical or Composite Blanking

The polarity of all of these signals is programmable; the signal names given above correspond the default settings of the polarity selection bits. The polarity selection bits are used as follows :

DCF.HPL = 1 $\quad \overline{\text{HSYNC}} \rightarrow \text{HSYNC}$

DCF.VPL = 1 $\quad \overline{\text{VSYNC}} \rightarrow \text{VSYNC}$

VCF.EOP = 1 $\quad \text{E/}\overline{\text{O}} \rightarrow \overline{\text{E}}\text{/O}$

DCF.BPL = 1 $\quad \overline{\text{HBLANK}} \rightarrow \text{HBLANK}, \ \overline{\text{VBLANK}} \rightarrow \text{VBLANK}$

VSYNC is mapped onto the register bit STA.VSY, and can be used to generate interrupt requests.

The source of video timing may be external or internal.

External Video Timing

If the video timing generator is external to the STi3400, then bit VCF.ENB must be reset. This is its default state. The video timing inputs required are $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ for horizontal and vertical synchronization, $\overline{\text{HBLANK}}$ for composite blanking, and E/$\overline{\text{O}}$ if it is required to output separate odd and even fields from the display buffer.

The start of each line is signalled by a falling edge of the $\overline{\text{HSYNC}}$ input. Internal pel (i.e. horizontal) counting is restarted by this event. $\overline{\text{HSYNC}}$ must be low for at least 4 PIXCLK cycles. The internal line counter is reset on the falling edge of $\overline{\text{VSYNC}}$, and incremented by the falling edge of $\overline{\text{HSYNC}}$. The state of the line counter at the start of the odd and even fields is shown in Figure 25. At the start of the odd field, $\overline{\text{VSYNC}}$ must fall at least 2 PIXCLK cycles before $\overline{\text{HSYNC}}$. The input signal E/$\overline{\text{O}}$, if used, must be valid before the $\overline{\text{HSYNC}}$ of the first line of active (non-background) video.

Internal Video Timing

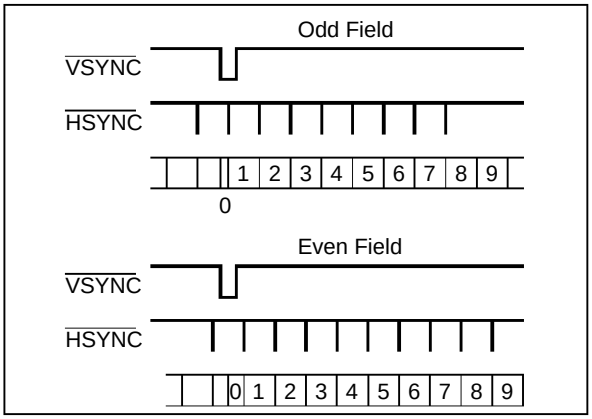
If the internal video timing generator (VTG) is used, then bit VCF.ENB must be set. The video timing outputs generated are $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ for horizontal and vertical synchronization, $\overline{\text{HBLANK}}$ and $\overline{\text{VBLANK}}$ for horizontal and vertical blanking. E/$\overline{\text{O}}$ indicates the field. VSYNC and VBLANK can be separately programmed to deliver composite synchronization and blanking, respectively.

Internal line counting is as shown in Figure 25.

Programming of the VTG is described in Section IX.5, "Video Timing Generator".

If bit CTL.ILC is set, then different lines are output from the displayed picture buffer in the odd and even fields, as defined by E/$\overline{\text{O}}$. During the odd field, lines 1, 3, 5, ... of the decoded picture are sent to the display, and during the even field lines 2, 4, 6, ... of the decoded picture are sent to the display. Note that the internal line count restarts every field. In the 525/60 standard, internal line count 1 in the odd field corresponds to display line 4, and internal line count 1 in the even field corresponds to display line 267. In the 625/50 standard, internal line count 1 in the odd field corresponds to display line 1, and internal line count 1 in the even field corresponds to display line 314.

Figure 25 : Internal Line Counting and External Synchronization



IX - DISPLAY FUNCTIONS (continued)

IX.3 - Setting Up the Display

The DFP register must be set up with the base address of the buffer containing the picture to be displayed. This register is double-buffered; when a new value is written it is taken into account on the occurrence of a VSYNC. Thus it is possible to write a new value of DFP every field, although it would normally be updated only once per frame.

The STi3400 has two built-in ways of displaying this data :

- Every line of the picture buffer is read starting on every VSYNC, i.e. scan is progressive. This mode would be used for example when displaying a picture which was decoded at half of the resolution of the display, and where it is necessary to use the same picture data for each field. It is selected by resetting bit CTL.ILC.
- Every second line of this data is read from the buffer. The reading of one of these fields is started on every VSYNC. If E/O indicates the odd field, the 1st, 3rd, 5th, etc. lines will be read. If E/O indicates the even field, then the 2nd, 4th, 6th, etc. lines will be read. This mode is selected by setting bit CTL.ILC.

If at any time no display is required, bit DCF.FBC may be reset, in which case the background colour, defined by BKC.R/Y[7:0], BKC.G/C_R[7:0] and DCF.B/C_B[7:0], is output.

The size and location of the display window is defined by the registers XDO, XDS, YDO and YDS. The values loaded into these registers define the horizontal and vertical boundaries of the displayed picture, as shown in Figure 26. Outside of the picture area the background colour is displayed.

Register YDO is loaded with the number of the last line of the top border, where lines are numbered as shown in Figure 25. With an interlaced display the same YDO value serves for both fields; the top line of the displayed picture will be in the odd field. Register YDS is loaded with a number defining the bottom line of displayed picture. With an interlaced display the same YDS value serves for both fields; the bottom line of the displayed picture will be in the even field. YDO and YDS are related as follows :

YDS - YDO = number of lines (in one field) in displayed picture

Register XDO is loaded with a number defining the last sample of the left-hand border, counted in units of PIXCLK cycles from the falling edge of HSYNC, according to the relation :

Last sample of left-hand border, XDO' = XDO + 5

where XDO' is the actual offset.

XDS is loaded with a number defining the last active sample in each line, counted in units of PIXCLK cycles from the falling edge of the signal HSYNC, according to the relation :

Last sample of active video, XDS' = XDS + 5

where XDS' is the actual offset.

The offset, XDO' cannot be less than 128 primary clock cycles. The user must calculate how many PIXCLK cycles are necessary to respect this constraint. Once the offset is reached the display unit will start delivering picture data even if VSYNC is still active.

If less than the whole decoded picture must be displayed, it is possible to define horizontal and vertical clipping values, as shown in Figure 26. Those parts of the picture which are clipped are displayed with the background colour.

Horizontal clipping, in units of PIXCLK periods, is defined by the value loaded in XYC.XC[5:0], according to the relation :

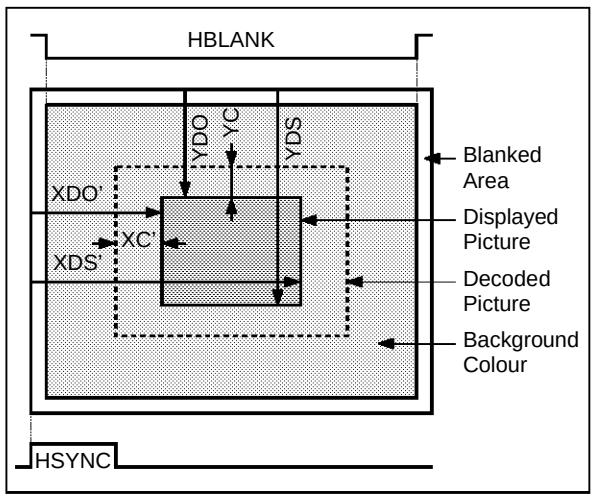
Horizontal clipping, XC' = 16 x (XYX.XC[5:0] + 1)

The clipping value is thus defined in units of macroblocks. The point at which the picture display starts is defined by XDO'. Clipping at the right-hand side of the picture is defined by the value chosen for XDS'.

Vertical clipping, in units of lines counted in each field, is defined directly by the value loaded in XYC.YC[9:0]. The line at which the picture display starts is defined by YDO. Clipping at the bottom of the picture is defined by the value chosen for YDS.

If the values chosen for the offsets and clipping values are such that the displayed picture would cross the boundary of the displayable area, as shown in Figure 26, the effective values of XDS' and YDS are the edges of the displayable area.

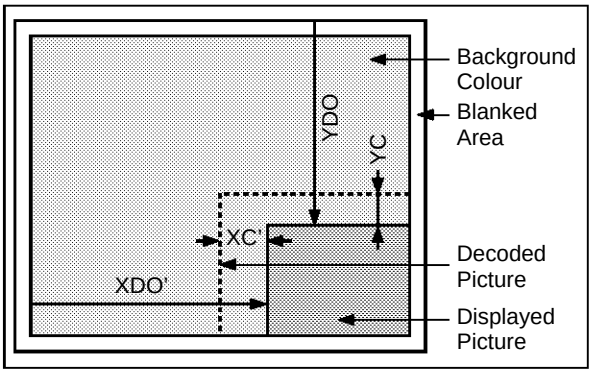
Figure 26 : Display Window Positioning (1)



IX - DISPLAY FUNCTIONS (continued)

The occurrence of HSYNC starts the output of another line, even if the previous one was not completed. Likewise the occurrence of VSYNC starts the output of a new picture, even if the previous one was not completed. This allows windows which lie outside the display area to be handled correctly.

Figure 27 : Display Window Positioning (2)



IX.4 - Reconstruction Modes

IX.4.1 - Chroma Reconstruction

The decoded picture is stored in the display buffer in 4:2:0 sampling format. For display this must be converted to 4:2:2 YC_BC_R format, or to 4:4:4 RGB format. In order to achieve this, additional chrominance samples must be constructed. These may either be created by duplication or by interpolation. In the latter case the vertical filter must be enabled.

If bit GCF.VCF is set, then vertical filtering is enabled, otherwise chrominance reconstruction is by duplication.

Figure 28 : 4:2:0 to 4:2:2 Conversion by Duplication of Chrominance Samples

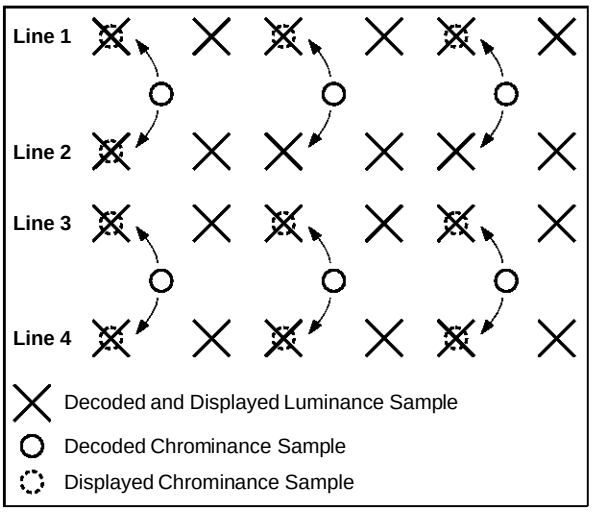
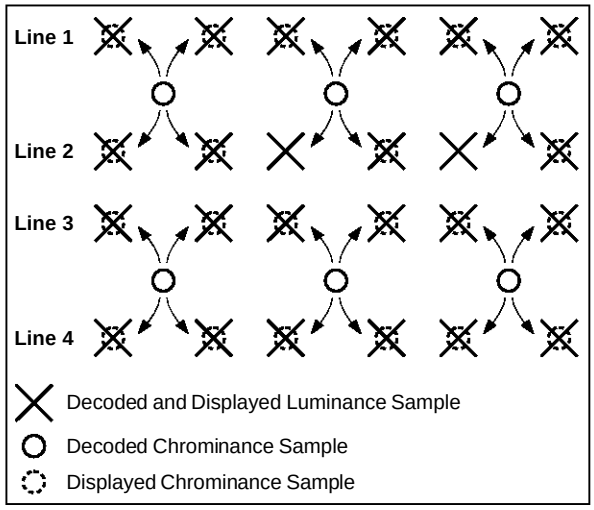


Figure 28 shows how the additional chrominance information required for 4:2:2 YC_BC_R output is created by duplication.

Figure 29 shows how the additional chrominance information required for 4:4:4 RGB output is created by duplication. The diagram shows how the additional colour difference samples are created before colour space conversion.

If the vertical filter is enabled, then the chrominance data is interpolated according to the rules given below. C(i) represents a chrominance sample on line i, after duplication in the manner of Figure 28 or Figure 29.

Figure 29 : 4:2:0 to 4:4:4 Conversion by Duplication of Chrominance Samples before Colour Space Conversion



The chrominance samples in a column are given by :

Line Number	Chroma Value
1	C(1)
2	C(2)
3	(C(2) + C(3))/2
4	C(4)
5	(C(4) + C(5))/2
6	C(6)
7	(C(6) + C(7))/2
8	C(8)
9	(C(8) + C(9))/2
10	C(10)

When vertical filtering is selected, the decoded picture width must not exceed 352 pels (22 macroblocks).

IX - DISPLAY FUNCTIONS (continued)

IX.4.2 - Horizontal Expansion

It is possible to double the number of pels in every line before outputting them to the display either by duplication or by filtering. Expansion is necessary for example when displaying CIF/SIF pictures on a 525/60 or 625/50 format interlaced display. In this case the same picture would be displayed in both fields.

A simple duplication of adjacent pels is performed when bit DCF.DUP is set. In this case one pair of colour difference samples serves four pels.

If bit XDO.EHF is set, then expansion is performed by the 8-tap horizontal filter, which acts on both luminance and chrominance data.

Bits DCF.DUP and XDO.EHF must not be set at the same time.

IX.5 - Video Timing Generator

The internal video timing generator (VTG) is enabled by setting bit VCF.ENB. Before enabling the VTG, all 5 words of the VCF register must be set up as defined in the VCF register description in Section XIII.2, "Register Descriptions".

There are two VTG modes of operation, Modes 0 and 1. In versions of the STi3400, in which the value returned after a read from REV = 00h, only Mode 0 is operational. In later versions, either Mode 0 or Mode 1 can be selected by the programming of bit VCF.MOD. The differences between the two modes are set out in the VCF register description in Section XIII.2, "Register Descriptions".

Mode 0 has been retained to enable compatibility with earlier versions of the STi3400. In new designs, only Mode 1 should be used.

After a hard reset, the VTG is disabled. Other types of reset have no effect on the VTG.

The effect of the various programming parameters on VTG output waveforms is shown in Figure 30, 31, 32, 33, 34 and 35.

IX.6 - Pel Output Rate

The maximum output rate (defined by the frequency of PIXCLK) is constrained firstly by the rate at which the STi3400 display FIFO can be filled from the memory and secondly by the maximum permissible frequency of PIXCLK. The display FIFO is sized to allow sustained pel output at rates up to 13.2MHz with a primary clock of 50MHz. This corresponds to the situation in which the display process is the only consumer of memory cycles apart from refresh. In any real application this rate will have to be reduced to comply with the memory bandwidth constraints specified in Section XI, "PERFORMANCE CALCULATION". With pixel expansion (duplication of filtering), the maximum sustained rate is twice this figure, i.e. 26.4MHz.

Higher rates of pel output are possible in burst mode. The burst rate calculation is given in Section XI, "PERFORMANCE CALCULATION".

Figure 30 : Horizontal Synchronization and Blanking

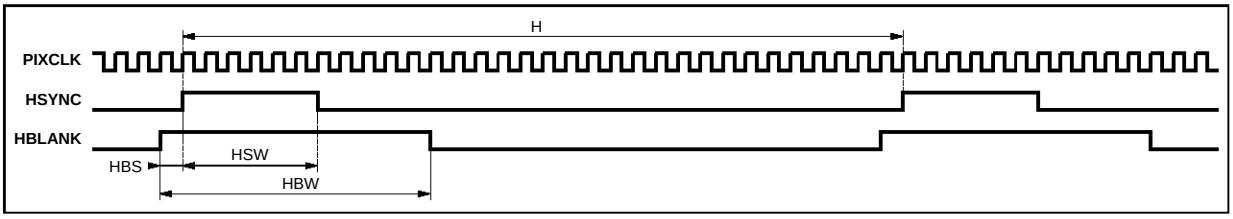
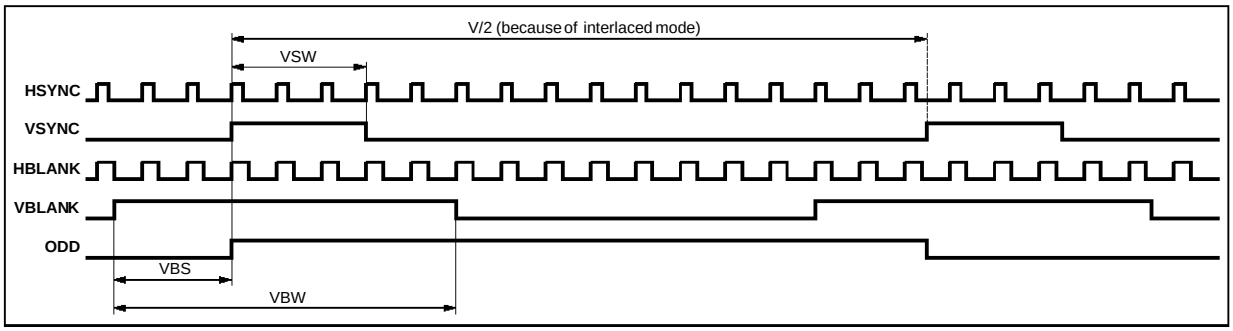


Figure 31 : Vertical Synchronization and Blanking (CPS = CPB = 0, INT = 1)



IX - DISPLAY FUNCTIONS (continued)

Figure 32 : Vertical Synchronization and Blanking (CPS = CPB = 1, INT = 1, EQU = 0, VSW is even)

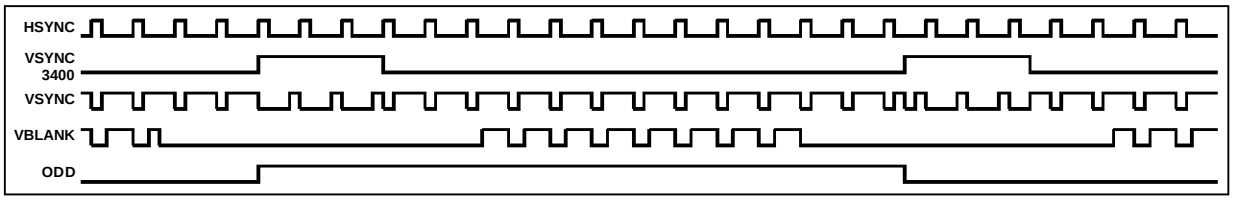


Figure 33 : Equalization and Serration Pulses (CPS = 1, INT = 1, EQU =1, VSW is odd)

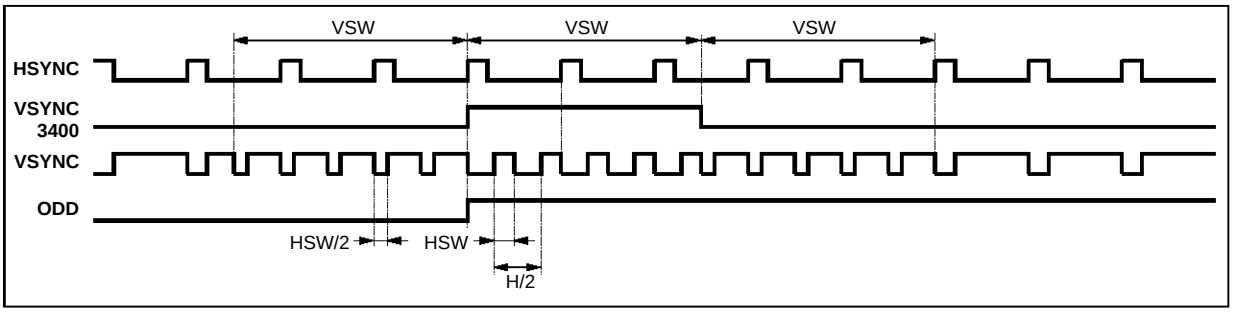


Figure 34 : Composite Blanking Pulses (CPB = CPS = 1, INT = 0, EQU = 1, VSW is odd)

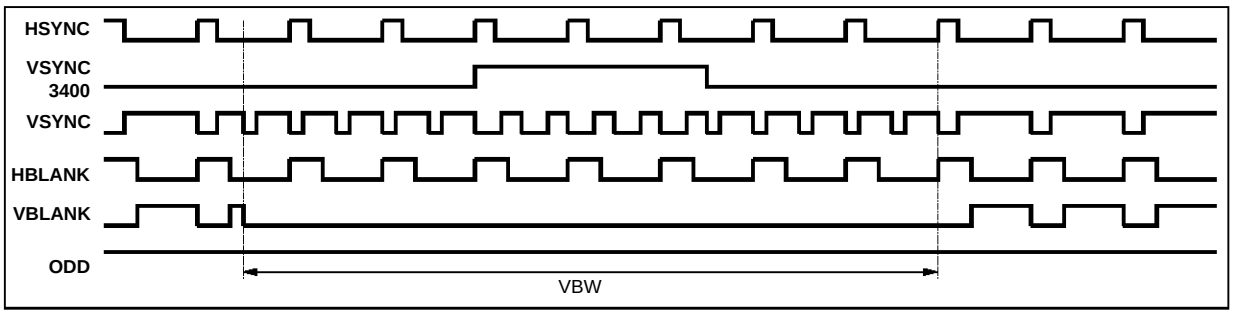
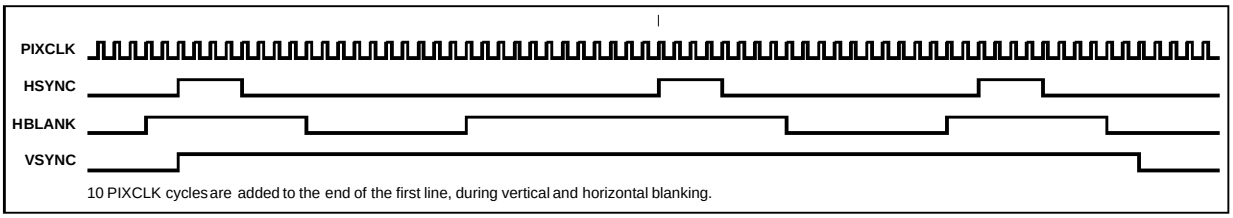


Figure 35 : Resynchronization Offset (DEL = 10)



X - CONTROL OF THE STi3400

Mainly derived from material already available in application notes. See also STi3240 Data Sheet.

XI - PERFORMANCE CALCULATION

This is essentially the same information as that given in the STi3240 Data Sheet.

XII - ELECTRICAL CHARACTERISTICS

XII.1 - Absolute Maximum Ratings

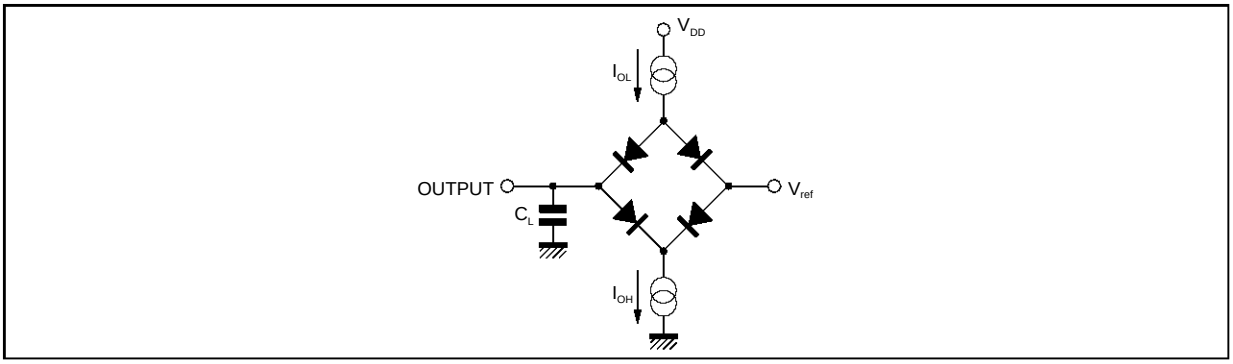
Symbol	Parameter	Value	Unit
V_{DD}	Power Supply	6	V
V_I, V_O	Voltages on Input and Output Pins	-1, V_{DD} + 0.5	V
T_{stg}	Storage Temperature	-65, +150	°C
T_{oper}	Ambient Operating Temperature	0, +70	°C

XII.2 - DC Electrical Characteristics (V_{DD} = 5V ±5%, T_{amb} = 0 to 70°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage		4.75		5.25	V
I_{DD}	Average Power Supply Current	C_{LOAD} = 50pF on all outputs $f_{primary}$ = 50MHz, all inputs at V_{DD} or 0V $f_{primary}$ = 0Hz			120 10	mA mA
V_{IL}	Input Logic Low Voltage (except CLK)				0.8	V
V_{IH}	Input Logic High Voltage (except CLK)		2			V
$V_{IL(CLK)}$	Input Logic Low Voltage (CLK)				0.6	V
$V_{IH\ (CLK)}$	Input Logic High Voltage (CLK)		2.5			V
	Input Leakage Current Inputs I/Os	V_{DD} = 5.25V, 0 ≤ V_{IN} ≤ V_{DD}	 -5 -1		 +5 +1	 µA µA
V_{OL}	Output Logic Low Voltage	V_{DD} = 5.25V, I_{LOAD} = 500µA			0.4	V
V_{OH}	Output Logic High Voltage	V_{DD} = 4.75V, I_{LOAD} = -500µA	4			V
C_{IN}	Input Capacitance	V_{offset} = 2.5V, f = 1MHz			10	pF

XII.3 - AC Electrical Characteristics (V_{DD} = 5V ±5%, T_{amb} = 0 to 70°C, unless otherwise specified)

Figure 36 : Test Load Circuit



Test Loads

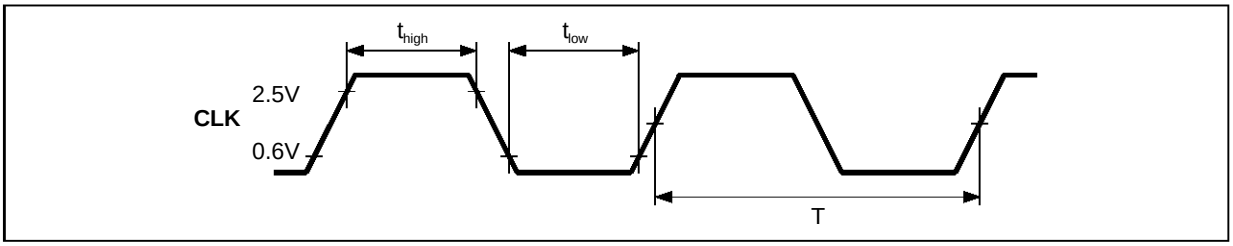
Output	I_{OL}	I_{OH}	C_L	V_{ref}
RY7-RY0, GC7-GC0, BC7-BC0, E/$\overline{O}$, VSYNC, VBLANK, HSYNC, HBLANK, D15-D0, CDREQ	500µA	500µA	50pF	1.5V
$\overline{DTACK}$, $\overline{IRQ}$, $\overline{DMAREQ}$	5mA	0	50pF	3.5V
$\overline{WE}$, $\overline{OE}$, $\overline{CAS}$	200µA	200µA	120pF	1.5V
AA8 - AA0	200µA	200µA	80pF	1.5V
$\overline{RAS3}$, $\overline{RAS0}$, DD15-DD0	200µA	200µA	30pF	1.5V

XII - ELECTRICAL CHARACTERISTICS (continued)

XII.3.1 - Primary Clock

Timings other than rise and fall times are specified with respect to a threshold of 1.5V

Figure 37 : Primary Clock



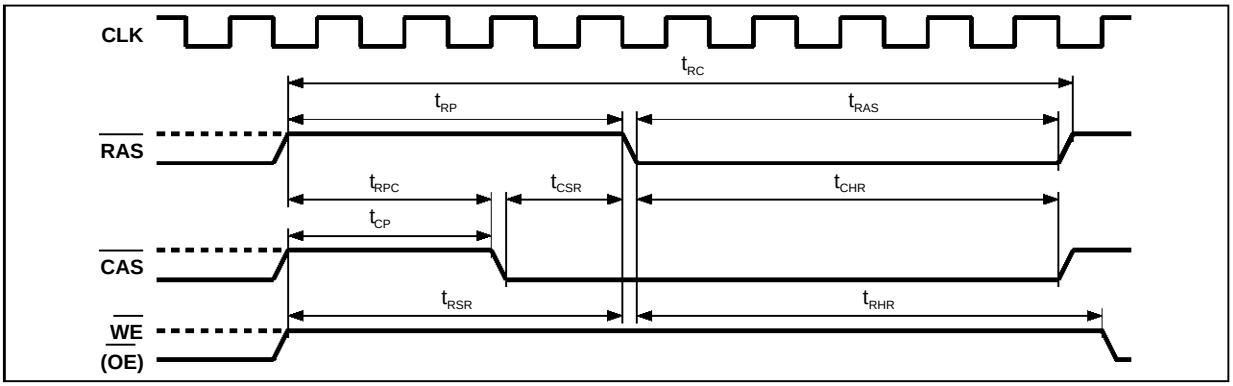
Symbol	Parameter	Min.	Typ.	Max.	Units
T	Primary Clock Period (see Note 1)	19.2			ns
t_{high}	Clock High Time	8			ns
t_{low}	Clock Low Time	8			ns
t_R, t_F	Clock Rise and Fall Time	2			ns

Note : 1. This corresponds to a maximum primary clock frequency of 52MHz.

XII.3.2 - DRAM Interface

All timing measurements are made with respect to thresholds of 0.8V and 2.4V.

Figure 38 : $\overline{CAS}$ Befor $\overline{RAS}$ Refresh Cycle (see Note 1)



Symbol	Parameter	Min.	Typ.	Max.	Units
t_{RC}	Cycle Time	9T			ns
t_{RP}	$\overline{RAS}$ Precharge Time	4T-10			ns
t_{RAS}	$\overline{RAS}$ Pulse Width	5T-10			ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time (see Note 2)	3T-10			ns
t_{CSR}	$\overline{CAS}$ to $\overline{RAS}$ Set-up Time	T-10			ns
t_{CHR}	$\overline{CAS}$ from $\overline{RAS}$ Hold Time (see Note 2)	5T-10			ns
t_{CP}	$\overline{CAS}$ Precharge Time	3T-10			ns
t_{RSR}	Read Command to $\overline{RAS}$ Set-up Time (see Note 3)	4T-10			ns
t_{RHR}	Read Command from $\overline{RAS}$ Hold Time (see Notes 4 and 5)	5T			ns

Notes :
1. T is the primary clock period.
2. Worst case is with one bank of memory.
3. Sometimes referred to as t_{WSR}.
4. Sometimes referred to as t_{WHR}.
5. Worst case is with one bank of memory.

XII - ELECTRICAL CHARACTERISTICS (continued)

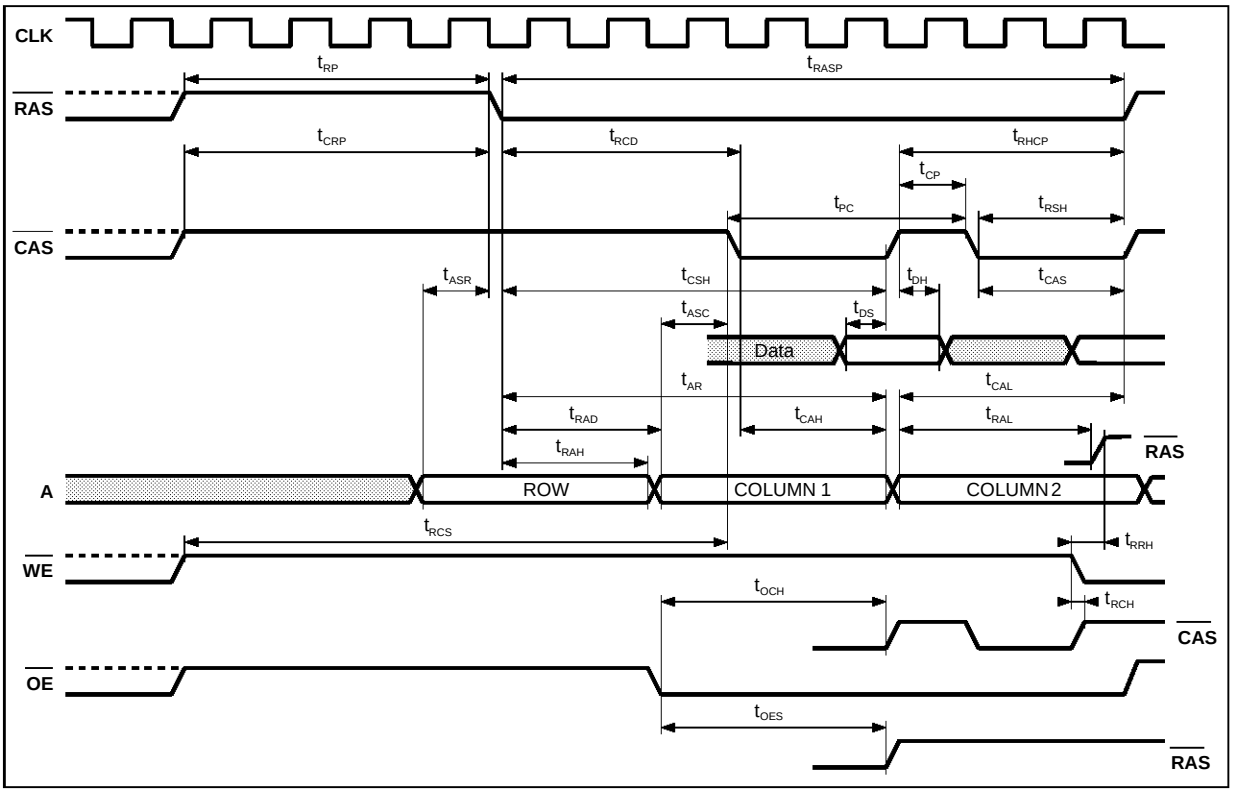
Page Mode Read Cycle (see Note 1)

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{RC}	Read Cycle Time	9T			ns
t_{RP}	$\overline{RAS}$ Precharge Time	4T-10			ns
t_{RASP}	$\overline{RAS}$ Pulse Width	5T-10			ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	4T-10			ns
t_{RCD}	$\overline{RAS}$ Low to $\overline{CAS}$ Low Delay Time (see Note 2)	3T-10			ns
t_{PC}	Fast Page Mode Read Cycle Time	3T-5			ns
t_{CP}	$\overline{CAS}$ Precharge Time	T-5			ns
t_{RHCP}	$\overline{RAS}$ Hold Time after $\overline{CAS}$ Precharge (see Note 3)	3T-5			ns
t_{RSH}	$\overline{RAS}$ Hold Time after $\overline{CAS}$	2T-8			ns
t_{CSH}	$\overline{CAS}$ Hold Time after $\overline{RAS}$ (see Note 2)	5T-10			ns
t_{CAS}	$\overline{CAS}$ Pulse Width	2T-8			ns
t_{ASR}	Row Address Set-up Time to $\overline{RAS}$	T-10			ns
t_{RAH}	Row Address Hold Time after $\overline{RAS}$ (see Note 4)	2T-5			ns
t_{ASC}	Column Address Set-up Time to $\overline{CAS}$ (see Note 5)	T-10			ns
t_{RAD}	Column Address Delay Time from $\overline{RAS}$ (see Note 4)	2T			ns
t_{CAH}	Column Address Hold Time from $\overline{CAS}$	2T-5			ns
t_{AR}	Column Address Hold Time from $\overline{RAS}$ (see Note 4)	5T-10			ns
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	3T-5			ns
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	3T-5			ns
t_{DS}	Data in Set-up Time to $\overline{CAS}$ Rising Edge	10			ns
t_{DH}	Data in Hold Time from $\overline{CAS}$ Rising Edge	5			ns
t_{RCS}	Read Command to $\overline{CAS}$ Set-up Time	7T-10			ns
t_{RCH}	Read Command from $\overline{CAS}$ Hold Time	3T-10			ns
t_{RRH}	Read Command from $\overline{RAS}$ Hold Time (see Note 6)	3T-10			ns
t_{OCH}	$\overline{CAS}$ from $\overline{OE}$ Hold Time	3T-5			ns
t_{OES}	$\overline{RAS}$ from $\overline{OE}$ Hold Time	3T-5			ns

Notes :
1. T is the primary clock period.
2. Worst case for min. value is with one bank of memory.
3. Sometimes referred to as t_{CPRH}.
4. Worst case is with two banks of memory.
5. Worst case is with two banks of memory.
6. Worst case is with one bank of memory.

XII - ELECTRICAL CHARACTERISTICS (continued)

Figure 39 : Page Mode Read Cycle



XII - ELECTRICAL CHARACTERISTICS (continued)

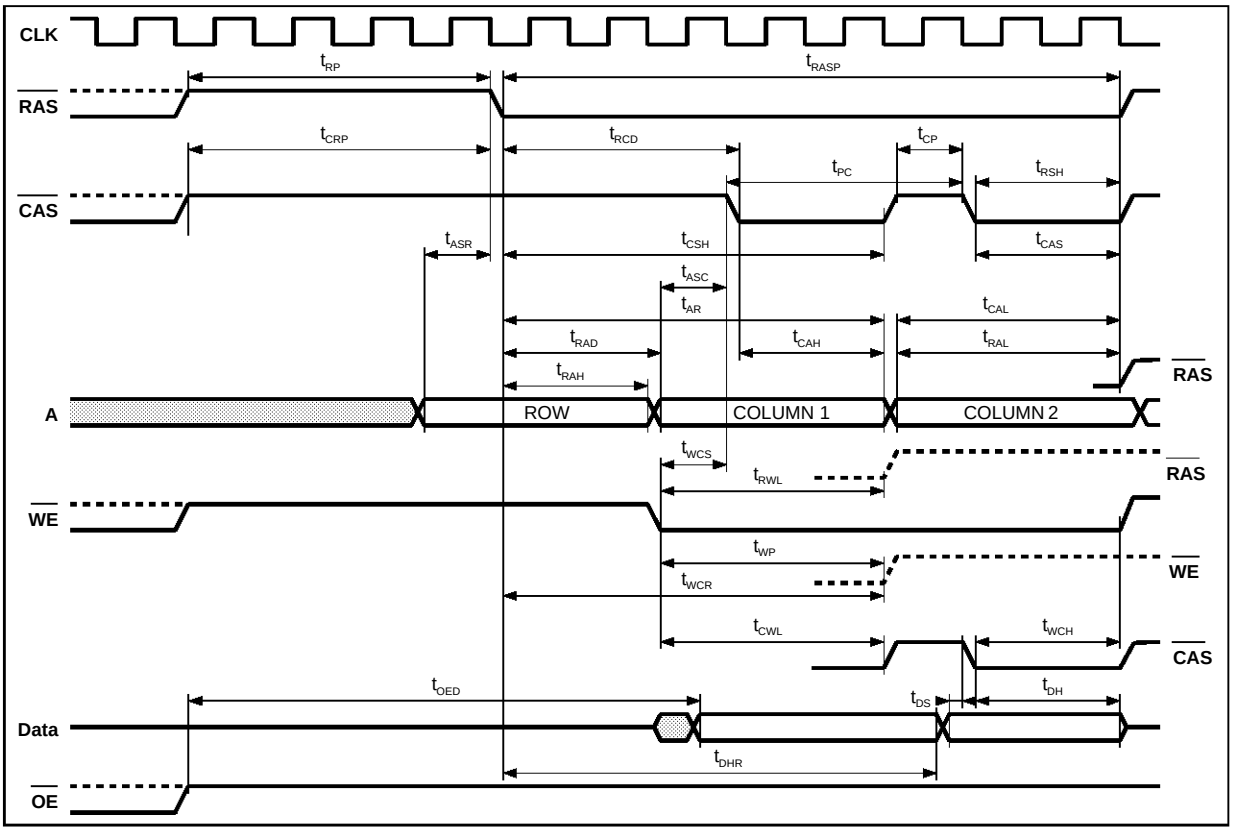
Page Mode Early Write Cycle (see Note 1)

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{RP}	$\overline{RAS}$ Precharge Time	4T-10			ns
t_{RASP}	$\overline{RAS}$ Pulse Width	5T-10			ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	4T-10			ns
t_{RCD}	$\overline{RAS}$ Low to $\overline{CAS}$ Low Delay Time (see Note 2)	3T-10			ns
t_{PC}	Fast Page Mode Read Cycle Time	3T-5			ns
t_{CP}	$\overline{CAS}$ Precharge Time	T-5			ns
t_{RSH}	$\overline{RAS}$ Hold Time after $\overline{CAS}$	2T-8			ns
t_{CSH}	$\overline{CAS}$ Hold Time after $\overline{RAS}$ (see Note 2)	5T-10			ns
t_{CAS}	$\overline{CAS}$ Pulse Width	2T-8			ns
t_{ASR}	Row Address Set-up Time to $\overline{RAS}$	T-10			ns
t_{RAH}	Row Address Hold Time after $\overline{RAS}$ (see Note 3)	2T-5			ns
t_{ASC}	Column Address Set-up Time to $\overline{CAS}$ (see Note 4)	T-10			ns
t_{RAD}	Column Address Delay Time from $\overline{RAS}$ (see Note 3)	2T			ns
t_{CAH}	Column Address Hold Time from $\overline{CAS}$	2T-5			ns
t_{AR}	Column Address Hold Time from $\overline{RAS}$ (see Note 3)	5T-10			ns
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	3T-5			ns
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	3T-5			ns
t_{WCS}	Write Command Set-up Time to $\overline{CAS}$	T-10			ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	3T-5			ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	3T-5			ns
t_{WCR}	Write Command Hold Time after $\overline{RAS}$ (see Note 5)	5T-10			ns
t_{WCH}	Write Command Hold Time after $\overline{CAS}$	3T-10			ns
t_{WP}	Write Command Pulse Width	3T-10			ns
t_{DS}	Data in Set-up Time to $\overline{CAS}$ Rising Edge	T-10			ns
t_{DH}	Data in Hold Time from $\overline{CAS}$ Rising Edge	2T-10			ns
t_{OED}	$\overline{OE}$ High before Data Valid	6T-10			ns
t_{OEH}	$\overline{OE}$ High Hold Time after Write Command ($\overline{WE}$ falling edge) (see Note 6)	9T-10			ns
t_{DHR}	Data Hold Time after $\overline{RAS}$ (see Note 4)	5T-10			ns

Notes :
1. T is the primary clock period.
2. Worst case for min. value is with one bank of memory.
3. Worst case for min. value is with one bank of memory.
4. Worst case is with two banks of memory.
5. Worst case is with one bank of memory.
6. Not shown on timing diagram.

XII - ELECTRICAL CHARACTERISTICS (continued)

Figure 40 : Page Mode Early Write Cycle

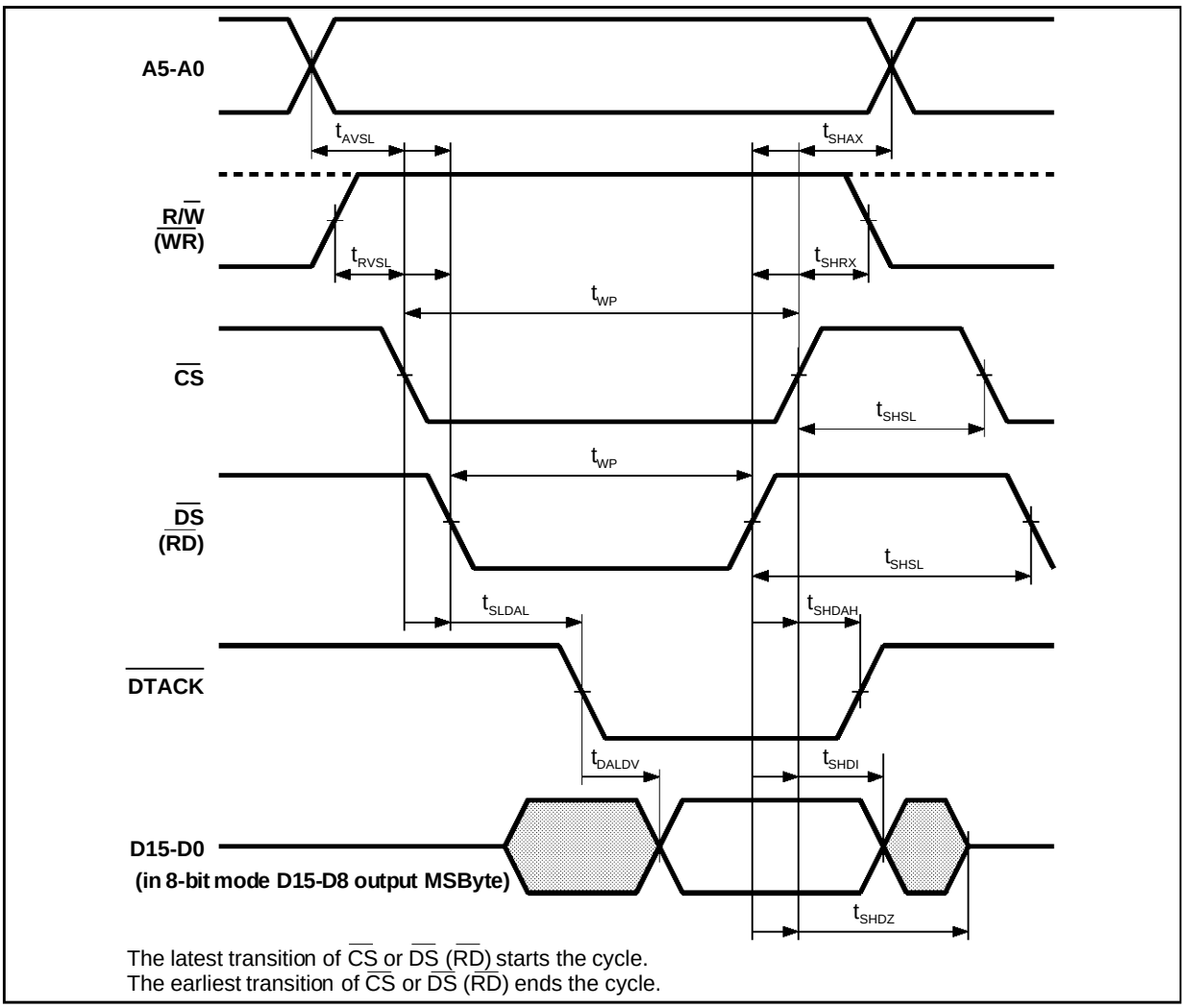


XII - ELECTRICAL CHARACTERISTICS (continued)

XII.3.3 - Microcontroller Interface

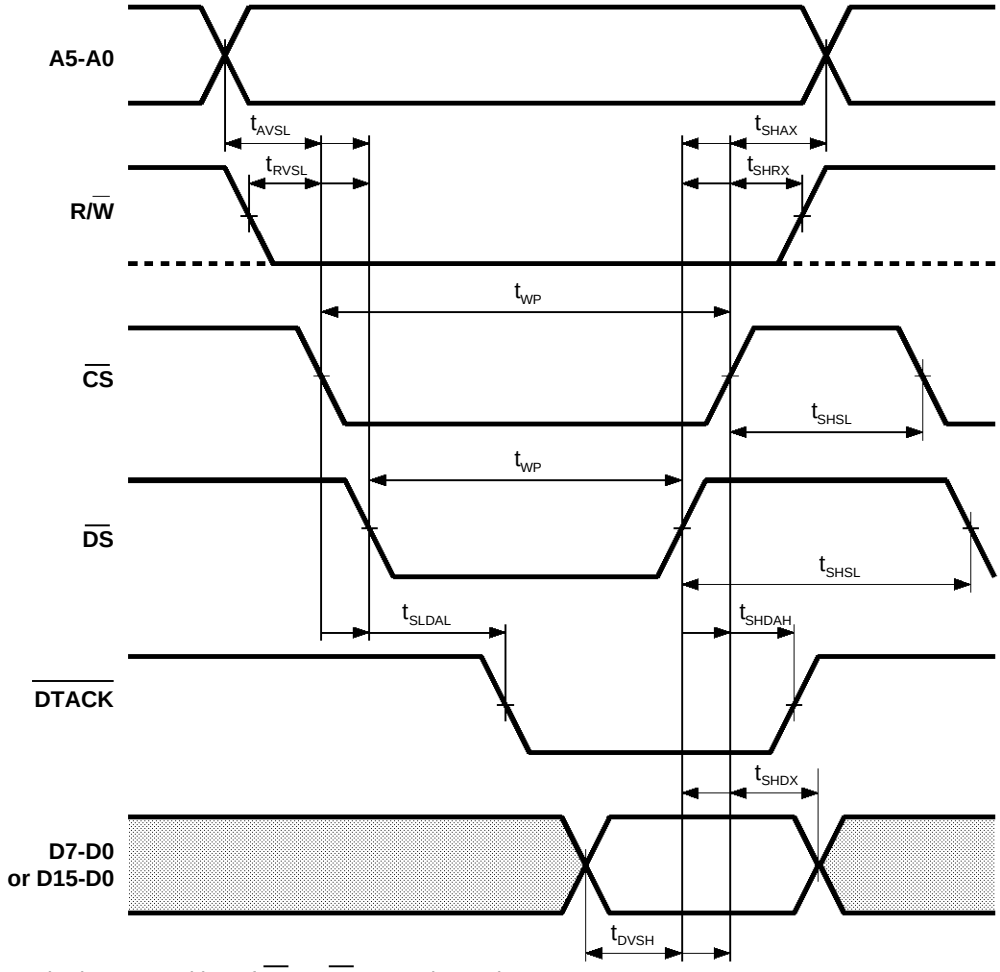
All timing measurements are made with respect to a threshold of 1.5V.

Figure 41 : Read Cycle Timing - Motorola and Intel Mode



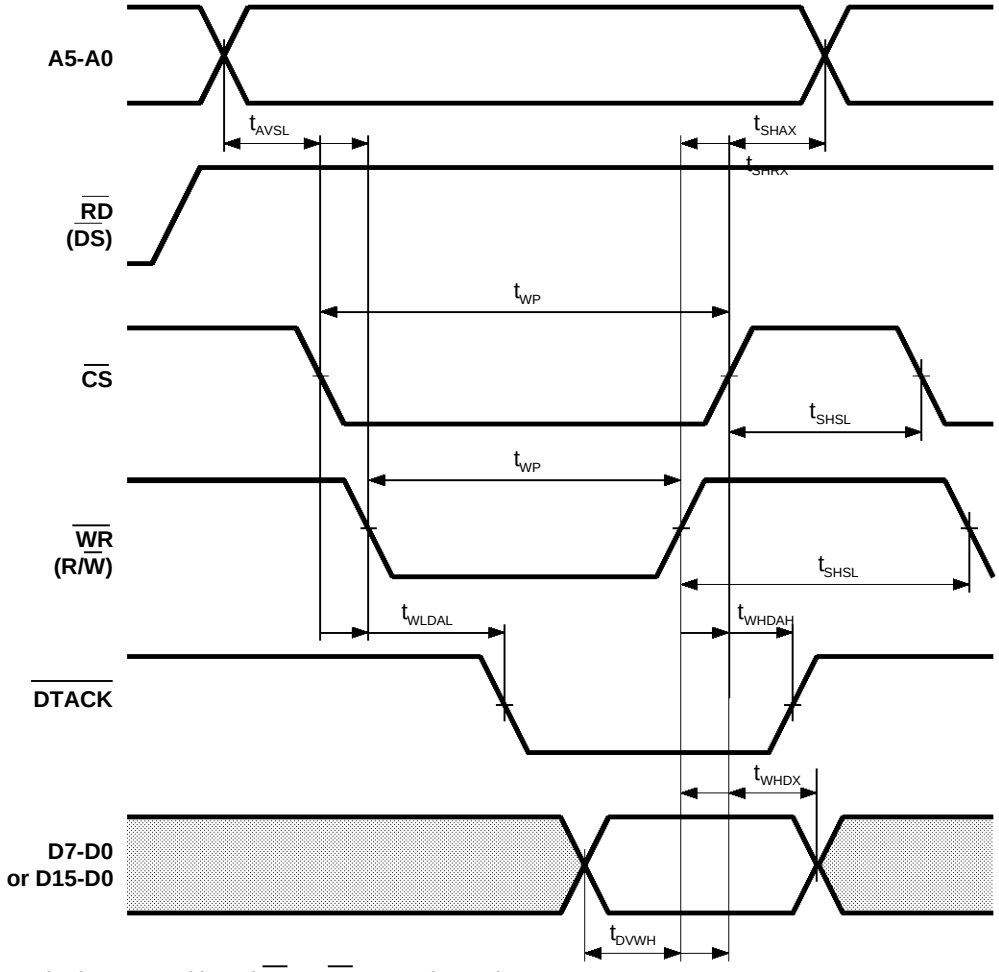
XII - ELECTRICAL CHARACTERISTICS (continued)

Figure 42 : Write Cycle Timing - Motorola Mode



XII - ELECTRICAL CHARACTERISTICS (continued)

Figure 43 : Write Cycle Timing - Intel Mode



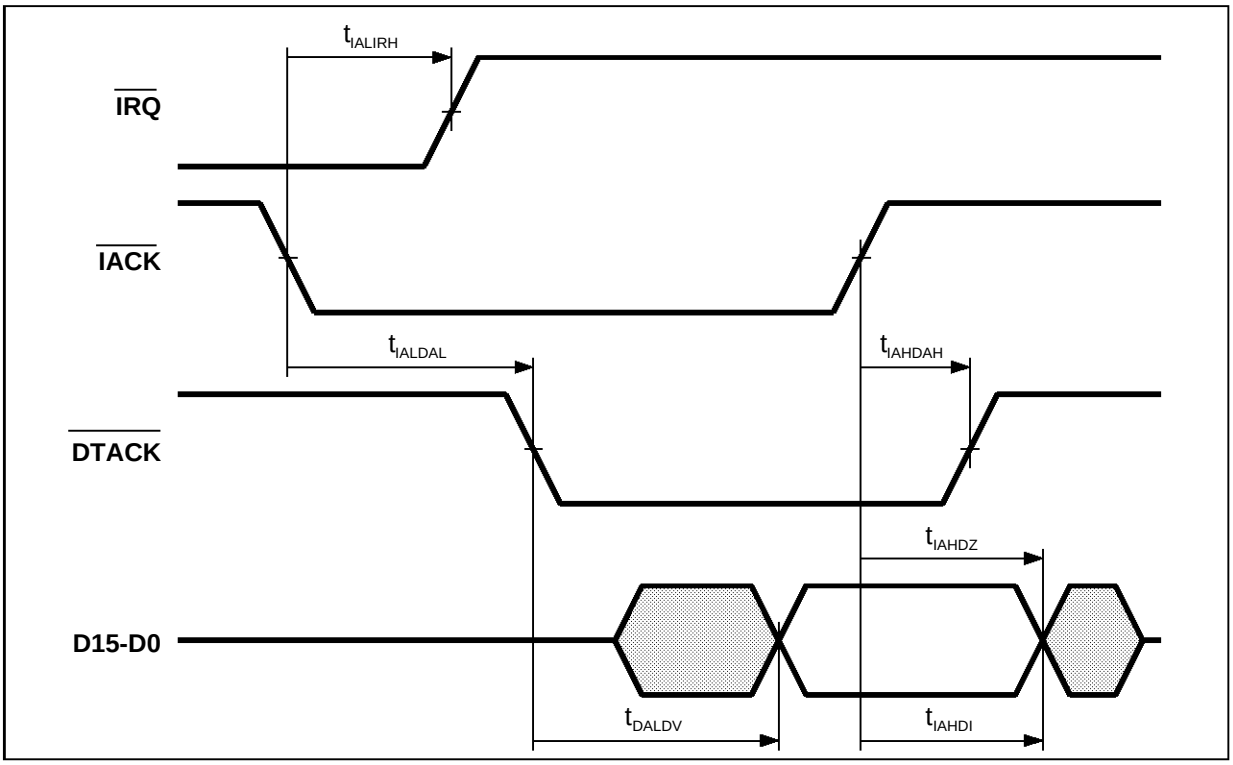
XII - ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{AVSL}	Address to $\overline{CS}$ or $\overline{DS}$/$\overline{RD}$/$\overline{WR}$ Low Set-up Time (See Note 1)	5			ns
t_{RVSL}	R/$\overline{W}$ to $\overline{CS}$ or $\overline{DS}$/$\overline{RD}$ Low Set-up Time (see Note 2)	5			ns
t_{SHAX}	Address from $\overline{CS}$ or $\overline{DS}$/$\overline{RD}$/$\overline{WR}$ High Hold Time (see Note 3)	5			ns
t_{SHRX}	R/W from $\overline{CS}$ or $\overline{DS}$ ($\overline{RD}$) High Hold Time (see Note 4)	5			ns
t_{WP}	$\overline{CS}$/$\overline{DS}$/$\overline{RD}$/$\overline{WR}$ Pulse Width (see Note 5)	50			ns
t_{SLDAL}	$\overline{CS}$ or $\overline{DS}$ ($\overline{RD}$) Low to $\overline{DTACK}$ Low (see Note 6)			45	ns
t_{WLDAL}	$\overline{WR}$ or $\overline{CS}$ Low to $\overline{DTACK}$ Low (see Note 7)			45	ns
t_{SHDAH}	$\overline{WR}$ or $\overline{CS}$ ($\overline{RD}$) High to $\overline{DTACK}$ High (see Note 8)			30	ns
t_{WHDAH}	$\overline{WR}$ or $\overline{CS}$ High to $\overline{DTACK}$ High (see Note 9)			10	ns
t_{SHSL}	$\overline{CS}$/$\overline{DS}$/$\overline{RD}$/$\overline{WR}$ High to Low Again	20			ns
t_{DALDV}	$\overline{DTACK}$ Low to Data Valid			15	ns
t_{SHDI}	$\overline{CS}$ or $\overline{DS}$ ($\overline{RD}$) High to Data Invalid	25			ns
t_{SHDZ}	$\overline{CS}$ or $\overline{DS}$ ($\overline{RD}$) High to Data Off (hi-Z)			20	ns
t_{DVSH}	Data Valid to $\overline{CS}$ or $\overline{DS}$ High Set-up Time	15			ns
t_{DVWH}	Data Valid to $\overline{WR}$ or $\overline{CS}$ High Set-up Time	15			ns
t_{SHDX}	Data from $\overline{CS}$ or $\overline{DS}$ High Hold Time	25			ns
t_{WHDX}	Data from $\overline{WR}$ or $\overline{CS}$ High Hold Time	25			ns

Notes :
1. Referenced to whichever of $\overline{CS}$, $\overline{DS}$, $\overline{RD}$ or $\overline{WR}$ changes last.
2. Referenced to whichever of $\overline{CS}$, $\overline{DS}$ or $\overline{RD}$ changes last.
3. Referenced from whichever of $\overline{CS}$, $\overline{DS}$, $\overline{RD}$ or $\overline{WR}$ changes first.
4. Referenced from whichever of $\overline{CS}$, $\overline{DS}$ or $\overline{RD}$ changes first.
5. Applies when $\overline{DTACK}$ is not used.
6. The latest transition of $\overline{CS}$ or $\overline{DS}$ ($\overline{RD}$) starts the cycle.
7. The latest transition of $\overline{WR}$ or $\overline{CS}$ starts the cycle.
8. The earliest transition of $\overline{CS}$ or $\overline{DS}$ ($\overline{RD}$) ends the cycle.
9. The earliest transition of $\overline{WR}$ or $\overline{CS}$ end the cycle.

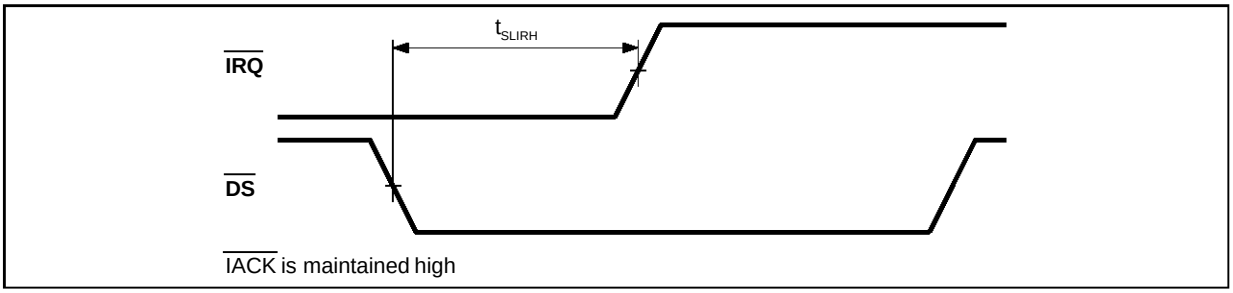
XII - ELECTRICAL CHARACTERISTICS (continued)

Figure 44 : Vectored Interrupt Acknowledge



Symbol	Parameter	Min.	Typ.	Max.	Units
t_{IALIRH}	$\overline{IACK}$ Low to $\overline{IRQ}$ High			25	ns
t_{IALDAL}	$\overline{IACK}$ Low to $\overline{DTACK}$ Low			30	ns
t_{DALDV}	$\overline{DTACK}$ Low to Interrupt Vector Valid			25	ns
t_{IAHDI}	$\overline{IACK}$ High to Interrupt Vector Invalid	20			ns
t_{IAHDZ}	$\overline{IACK}$ High to Data Bus High Impedance			20	ns
t_{IAHDAH}	$\overline{IACK}$ High to $\overline{DTACK}$ High			25	ns

Figure 45 : Non-Vectored Interrupt Acknowledge



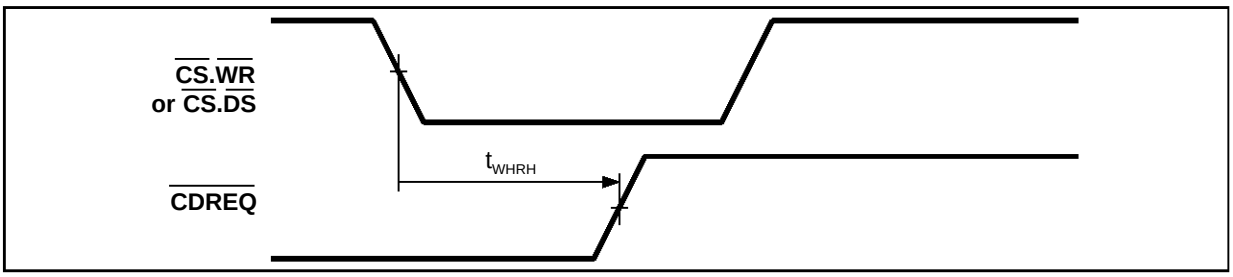
Symbol	Parameter	Min.	Typ.	Max.	Units
t_{SLIRH}	$\overline{DS}$ Low to $\overline{IRQ}$ High			10	ns

XII - ELECTRICAL CHARACTERISTICS (continued)

XII.3.4 - Compressed Data Input

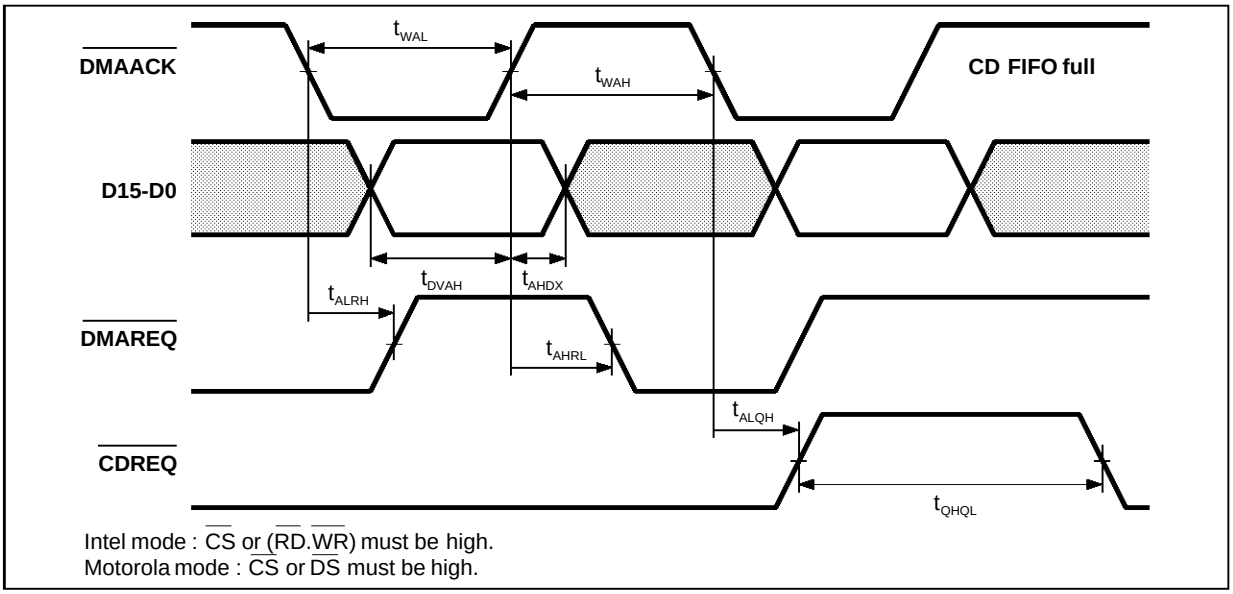
All timing measurements are made with respect to a threshold of 1.5V.

Figure 46 : $\overline{\text{CDREQ}}$ Delay from Programmed Write



Symbol	Parameter	Min.	Typ.	Max.	Units
t_{WHRH}	($\overline{CS}$ or $\overline{WR}$) High (Intel) or ($\overline{CS}$ or $\overline{DS}$) High (Motorola) to $\overline{CDREQ}$ High			40	ns

Figure 47 : DMA Transfer



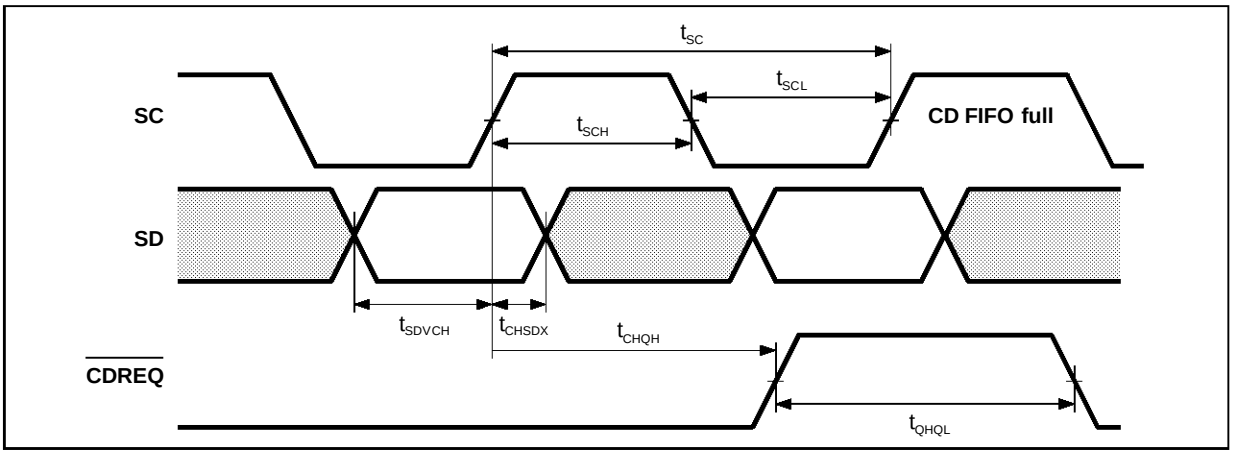
Intel mode : $\overline{CS}$ or ($\overline{RD}$.$\overline{WR}$) must be high.
Motorola mode : $\overline{CS}$ or $\overline{DS}$ must be high.

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{WAL}	$\overline{DMAACK}$ Width	35			ns
t_{WAH}	$\overline{DMAACK}$ High to Low Again	35			ns
t_{DVAH}	D15-D0 Set-up Time to $\overline{DMAACK}$ Rising Edge	30			ns
t_{AHDX}	D15-D0 Hold Time from $\overline{DMAACK}$ Rising Edge	0			ns
t_{ALRH}	$\overline{DMAACK}$ Low to $\overline{DMAREQ}$ High			35	ns
t_{AHRL}	$\overline{DMAACK}$ High to $\overline{DMAREQ}$ Low			25	ns
t_{ALQH}	$\overline{CDREQ}$ High from $\overline{DMAACK}$ Low (see Notes 1 and 2)			35	ns
t_{QHQL}	$\overline{CDREQ}$ High to Low Again			Primary Clock Cycles	

Notes : 1. $\overline{CDREQ}$ goes high if the write caused CD FIFO to become full.
2. For the CD FIFO to become empty there is a maximum delay of TBD primary clock cycles after the rising edge of $\overline{DMAACK}$.

XII - ELECTRICAL CHARACTERISTICS (continued)

Figure 48 : Serial Port CD Input



Symbol	Parameter	Min.		Max.	Units
t_{SC}	SC Period	50			ns
t_{SCH}	SC High Time	10			ns
t_{SCL}	SC Low Time	10			ns
t_{SDVCH}	SD Set-up Time to SC Rising Edge	20			ns
t_{CHSDX}	SD Hold Time from SC Rising Edge	5			ns
t_{CHQH}	$\overline{\text{CDREQ}}$ High from SC High (see Notes 1 and 2)			35	ns
t_{QHQL}	$\overline{\text{CDREQ}}$ High to Low Again	3T-5		Primary Clock Cycles	

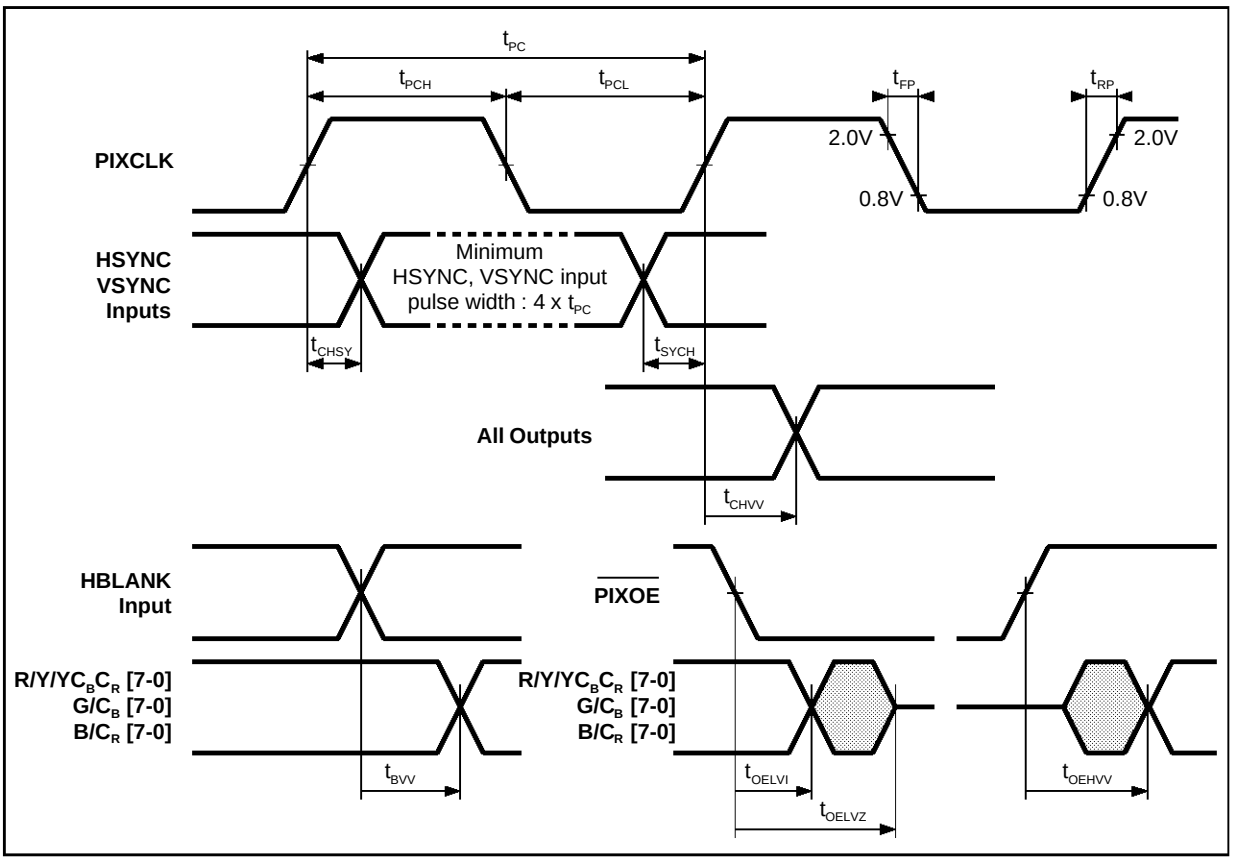
Notes : 1. $\overline{\text{CDREQ}}$ goes high if the write caused CD FIFO to become full. SC must stop after 16 more cycles if $\overline{\text{CDREQ}}$ remains high.
2. For the CD FIFO to become empty there is a maximum delay of TBD primary clock cycles after the rising edge of SC.

XII - ELECTRICAL CHARACTERISTICS (continued)

XII.3.5 - Video Interface Timing

All timing measurements are made with respect to a threshold of 1.5V.

Figure 49 : Video Interface

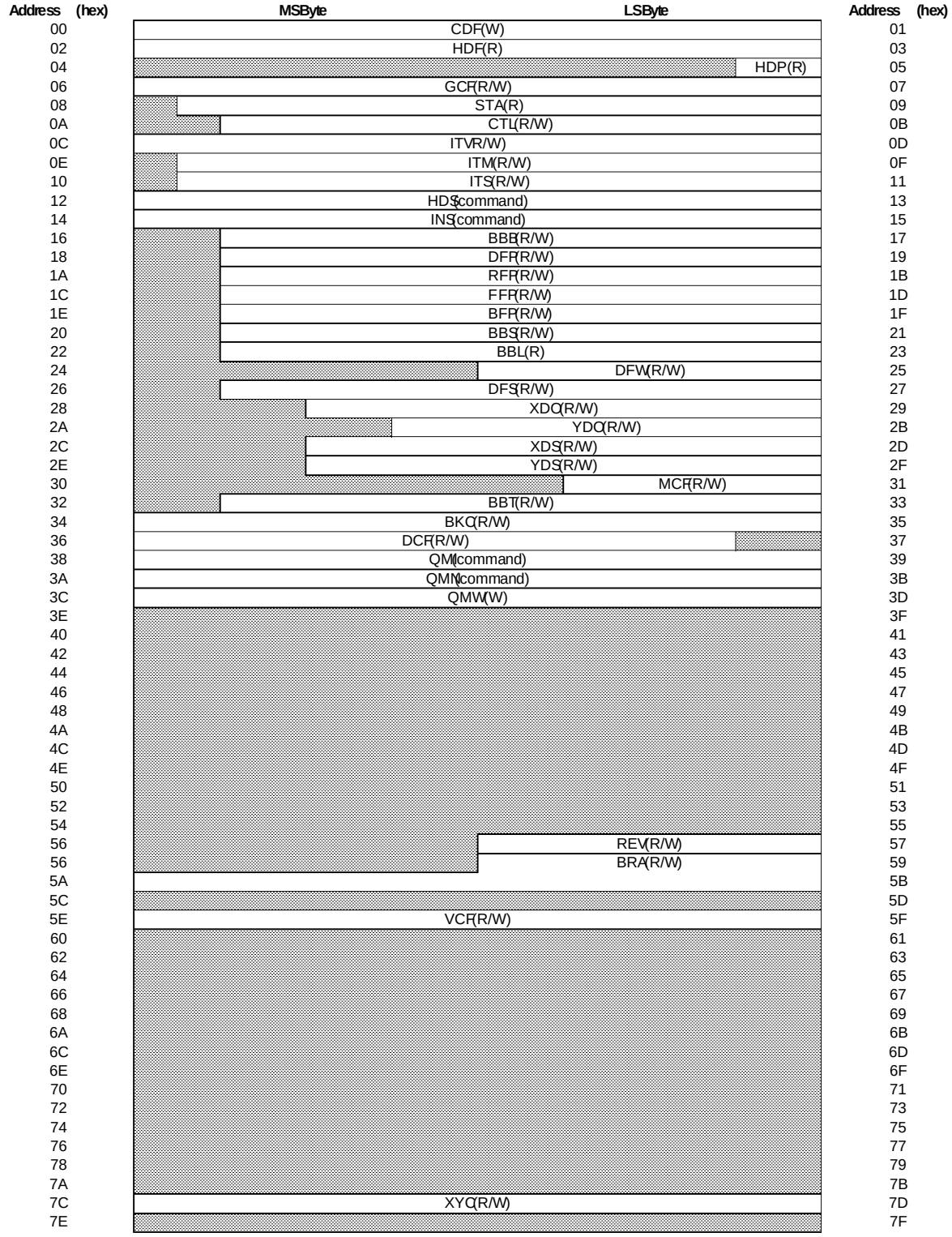


Symbol	Parameter	Min.	Typ.	Max.	Units
t_{PC}	Pel Clock Period for 8-bit Mode (see Note 1) Pel Clock Period for 16-bit or 24-bit Mode (see Note 2)	33.3 66.6			ns ns
t_{PCH}	Pel Clock High Time	13			ns
t_{PCL}	Pel Clock Low Time	13			ns
t_{RP}	Pel Clock Rise Time			3	ns
t_{FP}	Pel Clock Fall Time			3	ns
t_{CHSY}	HSYNC, VSYNC Set-up Time to PIXCLK Rising Edge (see Note 3)	25			ns
t_{SYCH}	HSYNC, VSYNC Hold Time from PIXCLK Rising Edge (see Note 3)	5			ns
t_{CHVV}	PIXCLK Rising Edge to Outputs RY, GC, BC All Others			10 10	ns ns
t_{BVV}	HBLANK to Video Output			30	
t_{OELVI}	$\overline{\text{PIXOE}}$ Low to Video Output Invalid			10	
t_{OELVZ}	$\overline{\text{PIXOE}}$ Low to Video Output High Impedance			20	
t_{OEHVV}	$\overline{\text{PIXOE}}$ High to Video Output Valid			35	

Note : 1. This corresponds to a PIXCLK frequency of 30MHz.
2. This corresponds to a PIXCLK frequency of 15MHz.
3. Minimum HSYNC, VSYNC input pulse width is 4 x t_{PC}.

XIII - REGISTERS

XIII.1 - Register Map



XIII - REGISTERS (continued)

XIII.2 - Register Descriptions

Registers are listed in alphabetical order.
All addresses are in hexadecimal.
All unspecified bits of the register map are reserved. Only the value 0 must be written to any of these bits. The values which are read from these bits are undefined.
The reset state is the state existing after a hard reset. Soft reset has no effect.

Synchronization

There are two types of register : synchronized and unsynchronized.

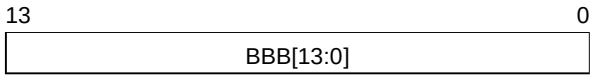
Synchronized registers only change value in response to an internal event, either DSYNC or VSYNC, depending on the register. These registers are double-banked ; during the write cycle the new value is loaded into a master register, and on the occurrence of the synchronizing event this value is loaded into a slave register, at which time the new value is available to the circuit. When reading a register synchronized by DSYNC or VSYNC, the value read back is the contents of the master register for BKC, DCF, INS, VCF, XDO, XDS, XYC, YDO, YDS, and the contents of the slave register for BFP, DFP, FFP and RFP.

Unsynchronized registers change their value immediately they are written to. With the exception of the CTL register, the unsynchronized registers are simple latches which are open during the whole of the write cycle. This constrains the mode of use of certain registers. Where this is the case it is stated in the descriptions below.

XIII - REGISTERS (continued)

XIII.2 - Register Descriptions (continued)

BBB - BIT BUFFER BOTTOM THRESHOLD

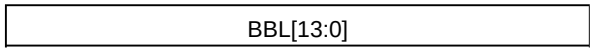


Address : 16-17
Type : R/W
Reset State : Undefined
Synchronization : None

Description

The register defined the level of fullness of the bit buffer below which STA.BBE becomes true. It is defined in units of 256 bytes.

BBL - BIT BUFFER LEVEL



Address : 22-23
Type : R
Reset State : 0 (also reset by a soft reset)

Description

This register indicates the current level of the bit buffer, defined in units of 256 bytes.
The value read is equal to :

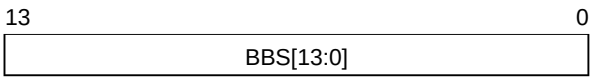
(bytes available - 64)/256.

When the microcontroller interface is in 8-bit mode, the bit buffer level may change between the reading of the two bytes.
The following procedure will ensure that the value read has consistent upper and lower bytes :

l1 ← BBL[7:0]
m ← BBL[13:8]
l2 ← BBL[7:0]
if l2 = l1 then level ← (m,l2)
else m ← BBL[13:8], level ← (m,l2)

This sequence should be protected from interruption.
When BBL is greater than the value held in the BBT register, the status bit STA.BBF becomes set. When BBL is zero, the status bit STA.BBE becomes set. These conditions can be used to generate interrupts.

BBS - BIT BUFFER SIZE

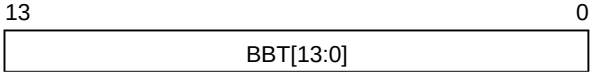


Address : 20-21
Type : R/W
Reset State : Undefined
Synchronization : None

Description

This register holds the address of the top of the bit buffer, defined in units of 256 bytes. The space allocated to the bit buffer starts at address 0.
BBS must only be changed before the first compressed data of a new sequence is input, and never during the decoding of a sequence.

BBT - BIT BUFFER TOP THRESHOLD



Address : 32-33
Type : R/W
Reset State : Undefined
Synchronization : None

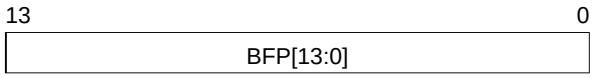
Description

This register holds the level of occupancy of the bit buffer, in units of 256 bytes, which when exceeded causes the status bit STA.BBF to become set, i.e. if BBL > BBT, STA.BBF is set. This threshold would normally be used to generate a "bit buffer nearly full" interrupt.
If the bit CTL.PBO is set, then transfer of data from the CD FIFO to the bit buffer is prevented if the bit buffer level is at or above the level defined in the BBT register. If BBT is set to a value equal to the top of the bit buffer, then this automatic mechanism will ensure than overflow never occurs.
If it is required to change the value of BBT during the decoding of a sequence, the input data D7 - D0 must be set-up not later than the start of the write cycle. This precaution will prevent false BBF interrupts.

XIII - REGISTERS (continued)

XIII.2 - Register Descriptions (continued)

BFP - BACKWARD PICTURE POINTER

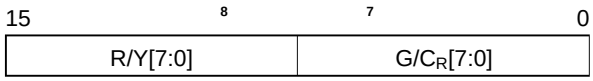


Address : 1E-1F
Type : R/W
Reset State : Undefined
Synchronization : DSYNC

Description

This register holds the start address of the backward prediction picture buffer, defined in units of 256 bytes.

BKC - BACKGROUND COLOUR



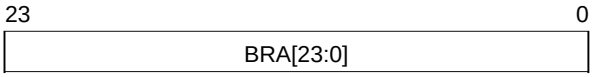
Address : 34-35
Type : R/W
Reset State : 0 (after first VSYNC)
Synchronization : VSYNC

Description

R/Y[7:0] The R component of the background colour if DCF.YUV = 0. The Y component of the background colour if DCF.YUV = 1.

G/C_R[7:0] The G component of the background colour if DCF.YUV = 0. The CR component of the background colour if DCF.YUV = 1.

BRA - BITSTREAM READ ADDRESS

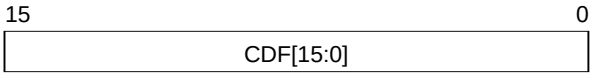


Address : 59-5A-5B
Type : R/W
Reset State : Undefined
Synchronization : None

Description

This register holds the number of 16-bit words, modulo 2^{24}, which have been read from the header FIFO.
This information can be used to keep track of time-stamps.

CDF - COMPRESSED DATA FIFO



Address : 00-01
Type : W
Reset State : Undefined
Synchronization : None (not a register)

Description

Writing to this register loads the next 16 bits of compressed data into the CD FIFO.
CDF[15] is 16 bits ahead of CDF[0] in the bitstream.

XIII - REGISTERS (continued)

XIII.2 - Register Descriptions (continued)

CTL - CONTROL

14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VMI	PRS	ERP	ERS	DRF	PBO	DVS	EEC	FIN	ERC	ILC	EDI	EVI	SRS	EDC

Address : 0A-0B
Type : R/W
Reset State : 0
Synchronization : End of write cycle

This is implemented a master-slave register in order to prevent problems of erroneous commands being issued during the write cycle.

Description

WMI Wait Mode after Instruction. If this bit is set, decoder automatically goes in wait mode after instruction is done. This prevents starting a new instruction if INS register is not updated.
Note : This bit only exists from version "DA".

PRS Pipeline Reset. In order to generate a pipeline reset, this bit must be set and reset by two successive writes. (the reset is generated by the detection of the 0 to 1 transition of PRS). The effect of a pipeline reset is that decoding of the current picture stops and the remaining bits are skipped until the next picture header is detected by the pipeline. At this point the pipeline enters the idle state.

ERP Enable Automatic Pipeline Reset on VLD or Pipeline Error.

ERS Enable Automatic Pipeline Reset on Severe Error.

DRF Disable Refresh. When this bit is set, automatic DRAM refresh is disabled. This must be done before switching control of the memory to another master.

PBO Prevent Bit Buffer Overflow. When this bit is set, bit buffer overflow (and thus the loss of data) is prevented by disabling the transfer of data from the compressed data FIFO to the bit buffer whenever the bit buffer level reaches the threshold defined in the BBT register.

DVS Disable VSYNC. When this bit is set VSYNC is prevented from starting the execution of a new instruction. It has no effect on the display process.

EEC Enable Automatic Error Concealment on VLD or Pipeline Error.

FIN Force Instruction. Setting and resetting of this bit forces execution of the next instruction. A DSYNC is generated. This should only be done when the pipeline is idle.

ERC Start Error Concealment. This bit, which must be set for a duration of at least 100 primary clock cycles (2µs if the clock is 50MHz), stops bitstream decoding and causes the pipeline to search for the next slice start code, at which point decoding resumes. The lost macroblocks are replaced using the rules given in Section VIII.6, "Error Recovery and Missing Macroblock Concealment".

ILC Interlaced Display. When this bit is set the odd lines (1, 3, 5...) of the displayed picture are output during the odd field, and the even lines (2, 4, 6...) are output during the even field.

EDI Enable DRAM Interface. When this bit is reset the DRAM interface (DD15-DD0, AA9-AA0, RAS3, RAS2, RAS1, RAS0, CAS, OE and WE) is put into its high impedance state. This bit must be set for normal operation.

EVI Enable Video Interface. When this bit is reset the video interface (RY7 -RY0, GC7-GC0, BC7-BC0) is put into its high impedance state. (It acts on the same outputs as the pin PIXOE). This bit must be set for normal operation.

SRS Soft Reset. In order to generate a soft reset, this bit must be kept set for a duration of at least 32 primary clock cycles (8µs if the clock is 50MHz). The effect of a soft reset is described in Section VI.1, "Resets".

EDC Enable Decoding. This bit must be set to allow decoding. No DSYNC signals are generated when this bit is reset.

XIII - REGISTERS (continued)

XIII.2 - Register Descriptions (continued)

DCF - DISPLAY CONFIGURATION

15 8	7	6	5	4	3	2	1	0
B/C_B[7:0]	HPL	VPL	BPL	DUP	YUV	FBC	BNK	V08

Address : 36-37
Type : R/W
Reset State : 0 (after first VSYNC)
Synchronization : VSYNC (only bits 2, 4, 8-15)

Description

B/C_B [7:0] The B component of the background colour if DCF.YUV = 0. The CB component of the background colour if DCF.YUV = 1.

DUP Pel Duplication. This bit selects the horizontal video out mode when the filter is not used (XDO.EHF = 0). This bit must not be set if XDO.EHF is set.
0 : No duplication.
1 : Duplication

YUV Output Colour Space. This selects RGB or YC_BC_R video output.
0 : RGB mode.
1 : YC_BC_R mode.

FBC Force Background Colour. When this bit is reset, only the background colour is output.
0 : Background colour only.
1 : Decoded picture window over background.

BNK Select Blank Level. This selects the video output level during blanking periods.

BNK	R, G, B	Y, C_B, C_R
0	0, 0, 0	0, 128, 128
1	16, 16, 16	16, 128, 128

V08 If set, select 8 bit multiplexed YC_BC_R output (27MHz)
Note : This bit is only exists from version "CA".

The function of bits HPL, VPL and BPL is dependent on the VTG mode.

In VTG mode 0 :

HPL HSYNC Polarity. This bit defines the polarity of the HSYNC pin on input or output.
0 : Input active low, output active high.
1 : Input active high, output active low.

VPL VSYNC Polarity. This bit defines the polarity of the VSYNC pin on input or output if bit VCF.CMP = 0. If VCF.CMP = 1, VSYNC output is composite sync and is always active high.
0 : Input active low, output active high.
1 : Input active high, output active low.

BPL BLANK Polarity. This bit defines the polarity of the HBLANK pin on input and output.
0 : Input active low, output active high.
1 : Input active high, output active low.
and of the VBLANK pin.
0 : Active high.
1 : Active low.
If VCF.CMP=1, VBLANK output is composite blank and is always active high.

In VTG mode 1 :

HPL HSYNC Polarity. This bit defines the polarity of the HSYNC pin on input or output.
0 : Active low.
1 : Active high.

VPL VSYNC Polarity. This bit defines the polarity of the VSYNC pin on input or output.
0 : Active low.
1 : Active high.

BPL BLANK Polarity. This bit defines the polarity of the HBLANK pin on input and output, and of the VBLANK pin.
0 : Active low.
1 : Active high.

DFP - DISPLAYED PICTURE POINTER

13 0
DFP[13:0]

Address : 18-19
Type : R/W
Reset State : Undefined
Synchronization : VSYNC

Description

This register holds the start address, defined in units of 256 bytes, of the picture which is currently being displayed. When a new value is written this is used when the next VSYNC occurs.
When DFP is set to same value as RFP (i.e. the decoder is writing the reconstructed picture into the buffer which is being displayed), bit INS.OVW must be set.

XIII - REGISTERS (continued)

XIII.2 - Register Descriptions (continued)

DFS - DECODED PICTURE SIZE

13															0
DFS[13:0]															

Address : 26-27
Type : R/W
Reset State : Undefined
Synchronization : None

Description

This register is set up with a value equal to the number of macroblocks in the decoded picture.
This is derived from the horizontal_size and vertical_size values transmitted in the MPEG sequence header, or if decoding in H.261 mode, to 396 for CIF picture format or 99 for QCIF picture format.
The maximum value is constrained by the amount of memory allocated to the picture buffers.

DFW - DECODED PICTURE WIDTH

7							0
DFW[7:0]							

Address : 24-25
Type : R/W
Reset State : Undefined
Synchronization : None

This register must only be written to between sequences when the decoder is in the idle state.

Description

This register is set up with a value equal to the width in macroblocks of the decoded picture.
This is derived from the horizontal_size value transmitted in the MPEG sequence header, or if decoding in H.261 mode, to 22 for CIF picture format or 11 for QCIF picture format.
The maximum value is 4080 (255 macroblocks).

FFP - FORWARD PICTURE POINTER

13															0
FFP[13:0]															

Address : 1C-1D
Type : R/W
Reset State : Undefined
Synchronization : DSYNC

Description

This register holds the start address of the forward prediction picture buffer, defined in units of 256 bytes.

GCF - GENERAL CONFIGURATION

15	14									6	5	4	3	2	1	0
DMA	RFI[8:0]										ME9	BSW	EVF	SER	CIF	H261

Address : 06-07
Type : R/W
Reset State : 0 (not reset by soft reset)
Synchronization : None

Description

DMA — Enable DMA. When this bit is set, the operation of the pin DMAACK is enabled.

RFI[8:0] — DRAM refresh interval in units of 3 primary clock periods. For example if each row in a 512-row memory must be refreshed every 8ms, with a primary clock of 50MHz, the following value must be stored in RFI[8:0] :
(8 x 10-3/512) x (50 x 106/3) → 260

ME9 — DRAM address bus width selection. This bit is set according to the type of DRAM used.
0 : Address bus width 10 bits.
1 : Address bus width 9 bits.

BSW — Enable CD port byte swap. If this bit is set, the MSByte and LSByte are switched internally when writing to the CD FIFO.

EVF — Enable vertical filter. If this bit is set, the chroma outputs are reconstructed by line averaging. If not, duplication is performed. The filtering option should only be selected when there are no more than 22 macroblocks per line.

SER — Serial port selection. This bit selects the compressed data input mode.
0 : Compressed data is input through the CDF register.
1 : Compressed data is input through the serial port.

CIF — H.261 picture format selection. This bit selects picture format when the decoder is operating in H.261 mode.
0 : QCIF.
1 : CIF.

H261 — Decoding mode. After performing a soft reset while in H.261 mode, this bit must be reset and then set again.
0 : MPEG.
1 : H.261.

XIII - REGISTERS (continued)

XIII.2 - Register Descriptions (continued)

HDF - HEADER DATA FIFO

15	0
HDF[15:0]	

Address : 02-03
Type : R
Reset State : Undefined

Description

When the start code detector has found a start code, the HDP register and then the header data FIFO, HDF, must be read in order to identify the start code. If header data is required, this can be obtained by further reads from HDF.

The start code identification procedure is described in Section VII.2, "Start Code Detection".

The word returned is a 16-bit slice of bitstream data.

If the microcontroller interface is in 8-bit mode, the MSByte must be read first.

The bitstream transmission order was HDF[15], HDF[14], ...

Before reading the header FIFO, status bit STA.HFE should be checked to ensure that it is not empty.

Bit STA.HFF set indicates that the header FIFO contains at least 16 words (256 bits) of data.

HDP - HEADER DATA POSITION

3	0
HDP[3:0]	

Address : 05
Type : R
Reset State : Undefined

Description

The data read from this register is used to indicate the position in the HDF register of a start code which has been detected by the start code detector.

It must be read before the first read from HDF.

MPEG Mode :

All start codes detected correspond to the bitstream pattern 000001XXh, where "XX" is the start code type, which can have any value except 01h through AFh (the slice start codes).

HDP[3:0] This indicates the position of the first bit of the start code type "XX" in the HDF register, counted from left to right. A value of zero indicates that HDF[15] is the first bit of the type. A value of 8 indicates that HDF[7] is the first bit of the type. When decoding an MPEG bitstream, the only possible values of HDP[3:0] are 0 and 8, since start codes are byte-aligned.

H.261 Mode :

The only start code detected, a picture start code, corresponds to the bitstream pattern "00010h".

HDP[3:0] This indicates the position of the first bit following the start code in the HDF register, counted from left to right. A value of zero indicates that HDF[15] is the first bit following the start code. A value of 15 indicates that HDF[0] is the first bit following the start code. When decoding an H.261 bitstream, all values of HDP[3:0] are possible.

HDS - HEADER DATA SEARCH

Address : 12-13
Type : Command
Synchronization : None (not a register)

Description

A write to this address launches a start code search by the start code detector. This is used to locate the first start code before the decoder is enabled, or when more than one start code must be found during a single task period (Start code detection is initiated automatically on every DSYNC).

XIII - REGISTERS (continued)

XIII.2 - Register Descriptions (continued)

INS - INSTRUCTION

15	14	13 10	9 6	5 4	3	2	1	0
OVW	QMS	BF[3:0]	FF[3:0]	PT[1,0]	SKP[0]	WAIT	RPT	SKP[1]

Address : 14-15
Type : R/W
Reset State : 0
Synchronization : "new instruction" (see Figure 22)

Description

This register contains the specification (the "instruction") for the next decoding task. The mechanism of instruction execution is described in Section VIII.4, "Decoding Task Control".

OVW Overwrite Mode. This bit must be set when the same picture buffer is used for both display and reconstruction. In this case, the decoder guarantees that the reconstruction never catches up with the display process. The overwrite mode must not be used if bit DCF.FBC (force background colour) is set.

QMS Quantizer Matrix Swap. When one or both of the quantization tables have been modified, this bit must be set in order to effect the swap of the modified table or tables. After a swap the tables are flagged as "unmodified" and cannot be swapped again until new table data has been written.

BF[3:0] Backward Vector Range and Resolution. When the next picture to be decoded is of type B, BF[3] is set equal to the full_pelbackward_vector parameter of the MPEG picture header, and BF[2:0] is set equal to backward_f_code of the MPEG picture header. This field is not used with other MPEG picture types, and when decoding in H.261 mode.

FF[3:0] Forward Vector Range and Resolution. FF[3] is set equal to the full_pelforward_vector parameter of the MPEG picture header, or to 1 if decoding in H.261 mode. FF[2:0] is set equal to forward_f_code of the MPEG picture header, or to 1 if decoding in H.261 mode.

PT[1:0] Picture Coding Type. When decoding in H.261 mode, PT[1,0] must be set to 2.

PT[1]	PT[0]	
0	0	Illegal
0	1	Intra (I)
1	0	Predictive (P)
1	1	Bidirectional (B)

SKP[1,0] Number of Pictures to be Skipped. (Note that SKP[1] is bit 0 and SKP[0] is bit 3).

SKP[1]	SKP[0]	
0	0	No Skipping
0	1	Skip 1 Picture
1	0	Skip 2 Pictures
1	1	Skip 3 Pictures

WAIT When this bit is set, no DSYNC is generated, i.e. no decoding task or start code detection is initiated.

RPT Repeat. When this bit is set, the task duration is defined to be two VSYNC periods, and pictures must be displayed twice. When this bit is reset, the task duration is one VSYNC period.

ITM - INTERRUPT MASK

14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SER	FLd	HFF	ESK	SST	PID	PER	VER	PSD	VSY	BBE	BBF	HFE	BFF	SCH

Address : 0E-0F
Type : R/W
Reset State : 0 (all interrupts disabled)
Synchronization : None

Description

Any bit set in this register will enable the corresponding interrupt.
An interrupt is generated whenever at bit in the STA register changes from 0 to 1 and the corresponding mask bit is set.

XIII - REGISTERS (continued)

XIII.2 - Register Descriptions (continued)

ITS - INTERRUPT STATUS

14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SER	FLD	HFF	ESK	SST	PID	PER	VER	PSD	VSY	BBE	BBF	HFE	BFF	SCH

Address : 10-11
Type : R
Reset State : Undefined

Description

When a bit in the STA register changes from 0 to 1, the corresponding bit in the ITS register is set, independent of the state of ITM.
If any ITS bit is unmasked, the signal $\overline{IRQ}$ is asserted.

A read of ITS clears the byte (or bytes) which were accessed. If the microcontroller interface is in 8-bit mode, the MSByte must be read first.
The interrupt request is removed after the reading of the LSByte.

ITV - INTERRUPT VECTOR

15	0
ITV[15:0]	

Address : 0C-0D
Type : R/W
Reset State : 0
Synchronization : None

Description

This register is loaded with the vector which is output in vectored interrupt mode.

MCF - MICRO INTERFACE CONFIGURATION

5	4	3	2	1	0
IRO	DMO	LBT	LCK	MOT	D16

Address : 30-31
Type : R/W
Reset State : 16-bit Motorola mode, unlocked, LBT = 0. Bit LBT is also reset by a soft reset. $\overline{IRQ}$ and DMAREQ open-drain.
Synchronization : None

Description

The micro interface configuration is changed by performing a sequence of reads from MCF, as defined in the state diagram of Figure 3. The value returned indicates the new configuration entered.

IRO Interrupt Request Open Drain.
0 : $\overline{IRQ}$ output is open-drain.
1 : IRQ output is totem-pole.

DMO DMA Request Open Drain.
0 : DMAREQ output is open-drain.
1 : DMAREQ output is totem-pole.

LBT Last CD Byte Written. When this bit is set it indicates that the last byte written to CDF has been sent to the CD FIFO, and is not still in the holding register. This information is required when using DMA transfer with the interface in 8-bit mode.

LCK Lock. Setting this bit locks the configuration of the micro interface, i.e. reading MCF cannot change the configuration.

MOT Motorola/Intel Mode.
0 : Intel mode.
1 : Motorola mode.

D16 Bus Width.
0 : 8-bit mode.
1 : 16-bit mode.

QMI - INITIALIZE INTRA Q TABLE

Address : 38-39
Type : Command
Synchronization : None (not a register)

Description

Before loading a intra quantization weighting table, a write to this address must be performed in order to reset the write pointer.

QMN - INITIALIZE NON-INTRA Q TABLE

Address : 3A-3B
Type : Command
Synchronization : None (not a register)

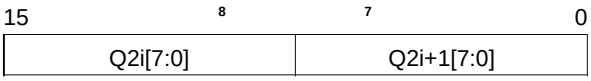
Description

Before loading a intra quantization weighting table, a write to this address must be performed in order to reset the write pointer.

XIII - REGISTERS (continued)

XIII.2 - Register Descriptions (continued)

QMW - QUANTIZATION MATRIX DATA



Address : 3C-3D
Type : W
Reset State : Undefined
Synchronization : None (not a register)

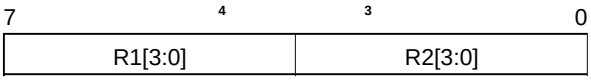
Description

To these addresses are written, starting at address 3C, the quantization coefficients in the order in which they appear in the bitstream, i.e. in zig-zag order. Which matrix (intra or non-intra) is written is determined by which of the commands QMI and QMN was executed last.

There are no built-in default quantization matrices.

Note : In H261 no matrix has to be loaded.

REV - REVISION REGISTER



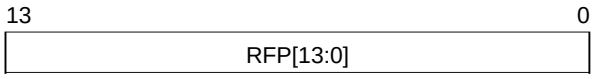
Address : 56-57
Type : R/W
Synchronization : None

Description

This register holds a two-digit code indicating the silicon revision. This code read corresponds to the first two characters of the revision code appearing on the package. For example for devices with the package code "X-CA1", the revision code CAh will be read. Before reading the code, 01 must be written to this register.

Note : In the earlier versions of the STi3400, this register is not present and the code "01" will be read.

RFP - RECONSTRUCTED PICTURE POINTER



Address : 1A-1B
Type : R/W
Reset State : Undefined
Synchronization : DSYNC

Description

This register holds the start address of the reconstructed (decoded) picture buffer, defined in units of 256 bytes.

XIII - REGISTERS (continued)

XIII.2 - Register Descriptions (continued)

STA - STATUS

14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SER	FLD	HFF	ESK	SST	PID	PER	VER	PSD	VSY	BBE	BBF	HFE	BFF	SCH

Address : 08-09
Type : R
Reset State : SER = 0
FLD = 0
HFF = 0
ESK = 0
SST = 0
PID = 1
PER = 0
VER = 0
PSD = 0
VSY = 0
BBE = 1
BBF = 0
HFE = 1
BFF = 0
SCH = 0

Description

This register contains a set of bits which represent the status of the decoder at any instant. Any change from 0 to 1 of any of these bits sets the corresponding bit of the ITS register, and can thus potentially cause an interrupt. STA.VSY and STA.PSD are pulses and are unlikely ever to be read as a 1.

The status bits have the following significance :

SER Severe Error. This bit is set when more than the programmed number of macroblocks (defined by DFS) have been decoded by the pipeline, either due to a bitstream or a programming error. If bit CTL.ERS is set, the decoding of the current picture will stop and the remainder of the bits will be skipped.

FLD Field Parity. This bit indicates the parity of the field currently being displayed. It may be used to generate an interrupt at the start of the odd field.
0 : even (field 2).
1 : odd (field 1).

HFF Header FIFO Full. This bit is set when the header FIFO contains at least 16 words (256 bits).

ESK End of Skipping. This bit is set when picture skipping has ended.

SST Slice/GOB Decoding Start. This bit is set when the decoding of a new slice or GOB has started.

PID Pipeline Idle. This bit is set when the STi3400 is not in the course of decoding a picture, i.e. when the pipeline is inactive. It becomes low when the decoding of a picture starts and high when picture decoding is complete. (It is also set at the end of each skipped picture, but should not be used to detect the end of skipping, since more than one picture could be skipped).

PER Pipeline Error. This bit is set when due to a data error, more than 64 coefficients are reconstructed in a block, or when more than 6 blocks are reconstructed in a macroblock. The decoding of the current picture stops. If bit CTL.EEC is set automatic error concealment will start.

VER VLD Error. This bit is set when the VLD detects a bitstream syntax error. The decoding of the current picture stops. If bit CTL.EEC is set automatic error concealment will start, and VER is reset. VER is also reset by a soft reset and by manual error concealment (bit CTL.ERC). It is not reset by a pipeline reset (bit CTL.PRS).

PSD Pipeline Starting to Decode. This bit is set for a short period (3 primary clock cycles) at the instant the pipeline starts decoding a picture. It is equivalent to DSYNC.

VSY VSYNC. This bit is set for a short time equal to the duration of the VSYNC signal.

BBE Bit Buffer Nearly Empty. This bit is set when the bit buffer level is below that defined by the BBB register.

BBF Bit Buffer Nearly Full. This bit is set when the bit buffer level is greater than that defined by the BBT register.

HFE Header FIFO Empty. This bit is set when the header FIFO has become empty after reading.

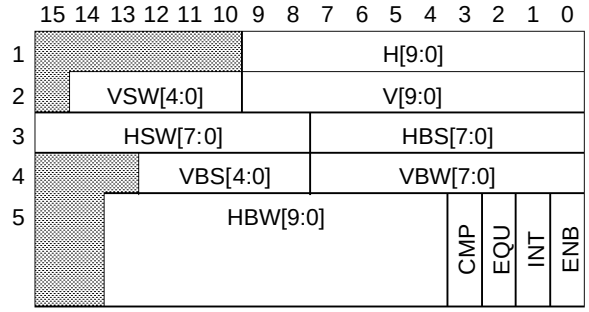
BFF Compressed Data (bitstream) FIFO Full. This bit is set when the CD FIFO is full. This bit is equivalent to the signal CDREQ.

SCH Start Code Hit. This bit is set whenever the first 16-bit word available in the header FIFO contains one the start codes recognized (see Section VII.2, "Start Code Detection"). While data is being read from the header FIFO, this bit can be tested to determine whether the next word contains a start code.

XIII - REGISTERS (continued)

XIII.2 - Register Descriptions (continued)

VCF - VIDEO TIMING GENERATOR CONFIGURATION (Mode 0)



Address : 5E-5F
Type : R/W
Reset State : All data 0, pointer set to word 1
Synchronization : VSYNC (but none for ENB)

Description

The VCF block of registers would generally be programmed as a unit. After a hard reset the register pointer is initialized, and register 1 is accessible. After a read or write the pointer will be incremented (modulo 5). In 8-bit mode, it is the access to the LSByte which causes the pointer to increment. To set up the VTG, 5 word writes are needed to this address.

H[9:0] Line Period. This is the line length, expressed in units of PIXCLK periods.

VSW[4:0] VSYNC Width. This is the pulse width of VSYNC, expressed in units of half-lines.

V[9:0] Number of lines in Frame. This would usually be set to 525 or 625.

HSW[7:0] HSYNC Width. This is the pulse width of HSYNC, expressed in units of PIXCLK periods.

HBS[7:0] HBLANK Lead Time. This is the time between the start of the HBLANK pulse and the start of the HSYNC pulse, expressed in units of PIXCLK periods.

VBS[4:0] VBLANK Lead Time. This is the time between the start of the VBLANK pulse and the start of the VSYNC pulse, expressed in units of half-lines.

VBW[7:0] VBLANK Width. This is the pulse width of VBLANK, expressed in units of half-lines.

HBW[9:0] HBLANK Width. This is the pulse width of HBLANK, expressed in units PIXCLK periods.

CMP Composite Sync and Blank. If this bit is set, the VSYNC and VBLANK pins deliver composite sync and blanking, respectively. (The HSYNC and HBLANK outputs are unaffected).

EQU Equalization. If this bit is set, equalization and serration pulses are present on the composite sync signal during frame synchronization.

INT Interlaced Mode. If this bit is set, synchronization pulses are generated for an interlaced display.

ENB Enable VTG. Setting this bit enables the internal video timing generator, and pins E/O, VSYNC, VBLANK, HSYNC and HBLANK become outputs. If it is reset, then external synchronization must be provided.

Examples

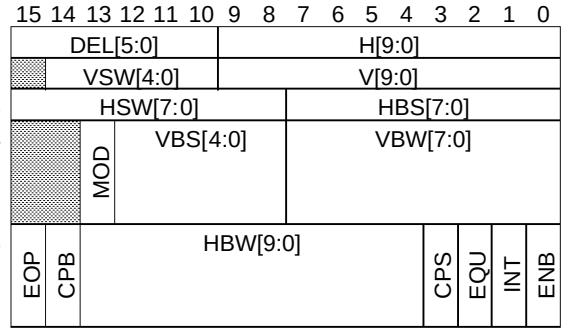
For a 625/50 display and a PIXCLK of 13.5MHz, the following values are needed :
H = 864, VSW = 5, V = 625, HSW = 64, HBS = 20, VBS = 5, VBW = 50, HBW = 160, EQU = 1, INT = 1

For a 525/60 display and a PIXCLK of 13.5MHz, the following values are needed :
H = 858, VSW = 6, V = 525, HSW = 64, HBS = 20, VBS = 6, VBW = 38, HBW = 154, EQU = 1, INT = 1

XIII - REGISTERS (continued)

XIII.2 - Register Descriptions (continued)

VCF - VIDEO TIMING GENERATOR CONFIGURATION (Mode 1)



Address : 5E-5F
Type : R/W
Reset State : All data 0, pointer set to word 1
Synchronization : VSYNC
(but none for EOP, ENB)

Description

The VCF block of registers would generally be programmed as a unit. After a hard reset the register pointer is initialized, and register 1 is accessible. After a read or write the pointer will be incremented (modulo 5). In 8-bit mode, it is the access to the LSByte which causes the pointer to increment. To set up the VTG, 5 word writes are needed to this address. If a VTG parameter, in particular DEL[5:0], needs to be changed while the VTG is running, register 5 should be read, not written, in order not to upset synchronization.
To change VTG values, first disable VTG, set-up new values and enable VTG.

DEL[5:0] Line1Delta. This is a 2's complement signed number which specifies an adjustment the length of line 1. The range of adjustments is -32 to 31 cycles of PIXCLK. This adjustment enables the decoder to keep in synchronization with the system clock reference.

H[9:0] Line Period. This is the line length, expressed in units of PIXCLK periods.

VSW[4:0] VSYNC Width. This is the pulse width of VSYNC, expressed in units of half-lines.

V[9:0] Number of lines in Frame. This would usually be set to 525 or 625.

HSW[7:0] HSYNC Width. This is the pulse width of HSYNC, expressed in units of PIXCLK periods.

HBS[7:0] HBLANK Lead Time. This is the time between the start of the HBLANK pulse and the start of the HSYNC pulse, expressed in units of PIXCLK periods.

MOD VTG Mode. This bit defines whether the VTG operates in Mode 0 or Mode 1. This bit is not programmable in versions of the STi3400 in which REV = 00h. These operate in Mode 0 only.
0 : VTG operates in Mode 0 (see previous VCF description).
1 : VTG operates in Mode 1 (according to this VCF description).

VBS[4:0] VBLANK Lead Time. This is the time between the start of the VBLANK pulse and the start of the VSYNC pulse, expressed in units of half-lines.

VBW[7:0] VBLANK Width. This is the pulse width of VBLANK, expressed in units of half-lines.

EOP E/O Polarity. This bit defines the polarity of the E/$\overline{O}$ pin on input or output.
0 : E/$\overline{O}$.
1 : $\overline{E}$/O.

CPB Composite Blanking. If this bit is set, the VBLANK pin delivers composite blanking. (The HBLANK output is unaffected).

HBW[9:0] HBLANK Width. This is the pulse width of HBLANK, expressed in units PIXCLK periods.

CPS Composite Sync. If this bit is set, the VSYNC pin delivers composite sync. (The HSYNC output is unaffected).

EQU Equalization. If this bit is set, equalization and serration pulses are present on the composite sync signal during frame synchronization.

INT Interlaced Mode. If this bit is set, synchronization pulses are generated for an interlaced display.

ENB Enable VTG. Setting this bit starts or restarts the internal video timing generator, and pins E/O, VSYNC, VBLANK, HSYNC and HBLANK become outputs. If it is reset, then external synchronization must be provided.

Examples

For a 625/50 display and a PIXCLK of 13.5MHz, the following values are needed :
H = 864, VSW = 5, V = 625, HSW = 64, HBS = 20, VBS = 5, VBW = 50, HBW = 160, EQU = 1, INT = 1

For a 525/60 display and a PIXCLK of 13.5MHz, the following values are needed :
H = 858, VSW = 6, V = 525, HSW = 64, HBS = 20, VBS = 6, VBW = 38, HBW = 154, EQU = 1, INT = 1

XIII - REGISTERS (continued)

XIII.2 - Register Descriptions (continued)

XDO - DISPLAY X OFFSET

12	11	10	9 ... 0
IFI	EHF	V24	XDO[9:0]

Address : 28-29
Type : R/W
Reset State : 0 (after first VSYNC)
Synchronization : VSYNC

Description

IFI Improved Filter. When set improved algorithm for SRC (Sample Rate Converter) is used. For better quality set IFI and EHF to enable filter.
Note : Not available prior to version "CA".

EHF Enable Horizontal Filter. When this bit is set the horizontal upsampling filter is enabled. When this bit is set, bit DCF.DUP (pel duplication) must be reset.

V24 24-bit YCRCB Output Format. This bit defines the video output format.

0 : is set, the video output mode is Y on pins RY7-RY0 and CB/CR multiplexed on pins BC7-BC0. If DCF.YUV is reset, the video output mode is R on pins RY7-RY0, G on pins GC7-GC0 and B on pins BC7-BC0.

1 : The video output mode is Y on pins RY7-RY0, CB on pins GC7-GC0, and CR on pins BC7-BC0. When this bit DCF.YUV (select YC_BC_R mode) must also be set.

XDO[9:0] This register is set up with a number defining the end of the right-hand border. This offset is measured from the active (first) edge of HSYNC and is specified in units of PIXCLK cycles. The value loaded into XDO[9:0] is equal to this offset minus 5. The largest offset which can be defined is therefore 1028.
Horizontal offset, XDO' = XDO + 5.
XDO programming is described in more detail in Section IX.3, "Setting up the Display".

XDS - DISPLAY X END

12 ... 0
XDS[12:0]

Address : 2C-2D
Type : R/W
Reset State : 0 (after first VSYNC)
Synchronization : VSYNC

Description

This register is set up with a number defining the right-hand boundary of the display window, expressed in units of PIXCLK cycles. The value of XDS[12:0] must be equal to XDO.XDO[9:0] plus the width of the display window. The actual offset, XDS', is thus equal to XDO + 5. XDS programming is described in Section IX.3, "Setting up the Display".

XYC - DISPLAYED PICTURE CLIPPING

15 ... 10	9 ... 0
XC[5:0]	YC[9:0]

Address : 7C-7D
Type : R/W
Reset State : XC = 3Fh, YC = 0 (after first VSYNC)
Synchronization : VSYNC

Description

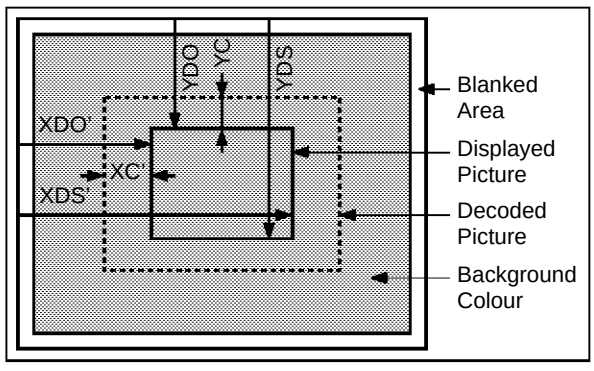
This register define which part of the decoded picture is displayed within the display window (defined by XDO, XDS, YDO, YDS). Those parts which are clipped are displayed with the background colour.

XC[5:0] Horizontal Clipping Value. The horizontal clipping, defined in units of PIXCLK periods is given by :
Horizontal clipping, XC' = 16 x (XC + 1).

YC[9:0] Vertical Clipping Value. This defines directly the vertical clipping, in units of lines.

The interpretation of the clipping values is shown in Figure 50. XYC programming is described in more detail in Section IX.3, "Setting up the Display".

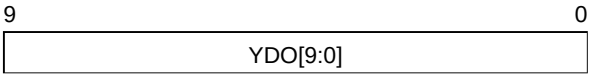
Figure 50 : Use of XC and YC



XIII - REGISTERS (continued)

XIII.2 - Register Descriptions (continued)

YDO - DISPLAY Y OFFSET



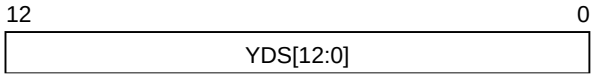
Address : 2A-2B
Type : R/W
Reset State : 0 (after first VSYNC)
Synchronization : VSYNC

Description

This register is set up with a number defining the last line of the upper border of the display, i.e. the top edge of the display window. Lines are counted from the active (first) edge of VSYNC. In an interlaced display, the same value of YDO would be used for both fields.

YDO programming is described in Section IX.3, ”Setting up the Display”.

YDS - DISPLAY Y END



Address : 2E-2F
Type : R/W
Reset State : 0 (after first VSYNC)
Synchronization : VSYNC

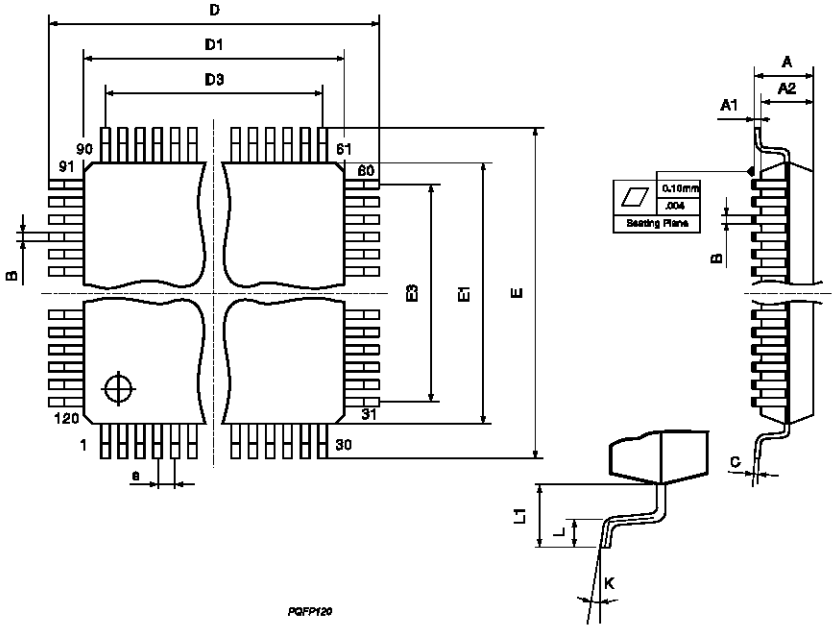
Description

This register is set up with a number defining the bottom line of the display window. The value of YDS[12:0] must be equal to YDO[9:0] plus the number of lines, counted in one field, in the display window. In an interlaced display, the same value of YDO would be used for both fields.

YDS programming is described in Section IX.3, ”Setting up the Display”.

PACKAGE MECHANICAL DATA

160 PINS - PLASTIC QUAD FLAT PACK



PMPQF120.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			4.07			0.160
A1	0.25			0.010		
A2	3.17	3.42	3.67	0.125	0.135	0.145
B	0.30		0.45	0.012		0.018
C	0.13		0.23	0.005		0.009
D	30.95	31.20	31.45	1.218	1.228	1.238
D1	27.90	28.00	28.10	1.098	1.102	1.106
D3		23.20			0.913	
e		0.80			0.031	
E	30.95	31.20	31.45	1.218	1.228	1.238
E1	27.90	28.00	28.10	1.098	1.102	1.106
E3		23.20			0.913	
L	0.65	0.80	0.95	0.026	0.0315	0.0374
L1		1.60			0.063	
K	0^o (Min.), 7^o (Max.)					

PQFP120.TBL